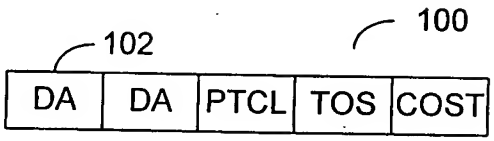


FIG. 1

200

```
If DA=DA1, SA=SA1, and TOS=TOS1                    } 203
  then select RI2
  else if DA=DA1 and SA=SA1                        } 202
     then select RI1
     else if DA=DA1                                } 201
        then select RI0
     endif
  endif
endif
```

FIG. 2

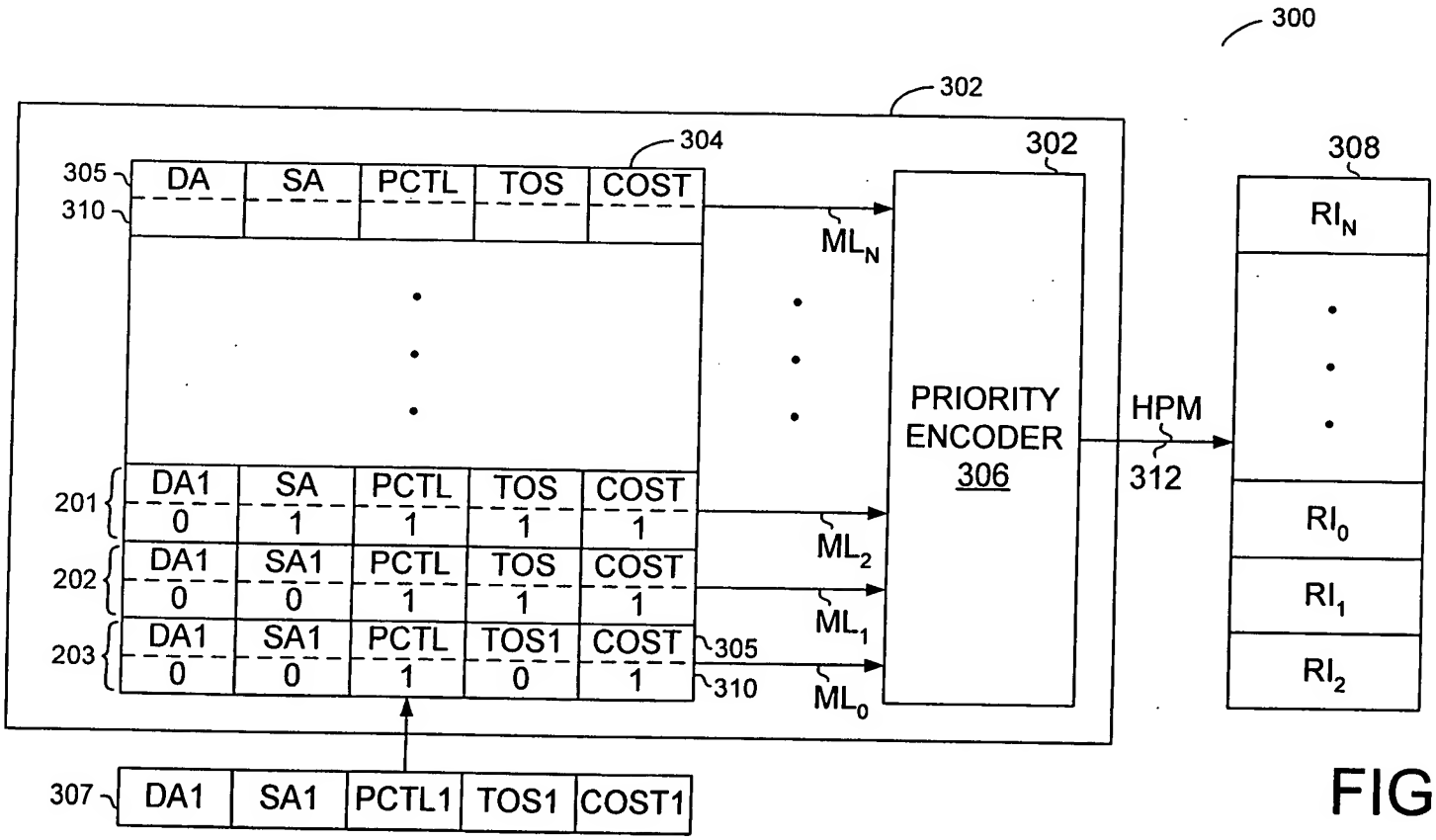


FIG. 3

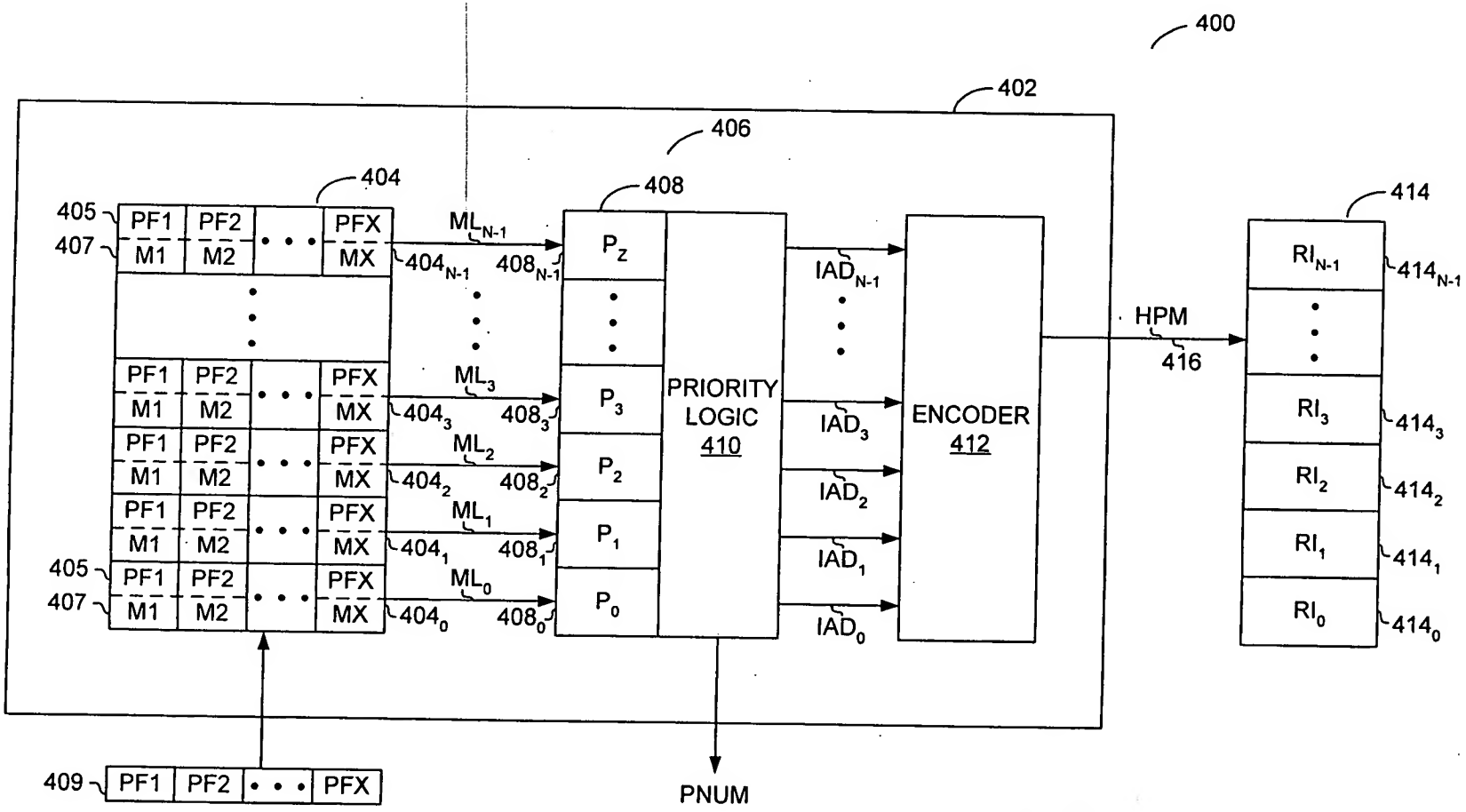

400
402
406
404
408
414
405
407
PF1
PF2
PFX
M1
M2
MX
ML_{N-1}
ML_3
ML_2
ML_1
ML_0
404_{N-1}
404_3
404_2
404_1
404_0
408_{N-1}
408_3
408_2
408_1
408_0
P_Z
P_3
P_2
P_1
P_0
PRIORITY LOGIC 410
IAD_{N-1}
IAD_3
IAD_2
IAD_1
IAD_0
ENCODER 412
HPM
416
RI_{N-1}
RI_3
RI_2
RI_1
RI_0
414_{N-1}
414_3
414_2
414_1
414_0
409
PNUM

FIG. 4

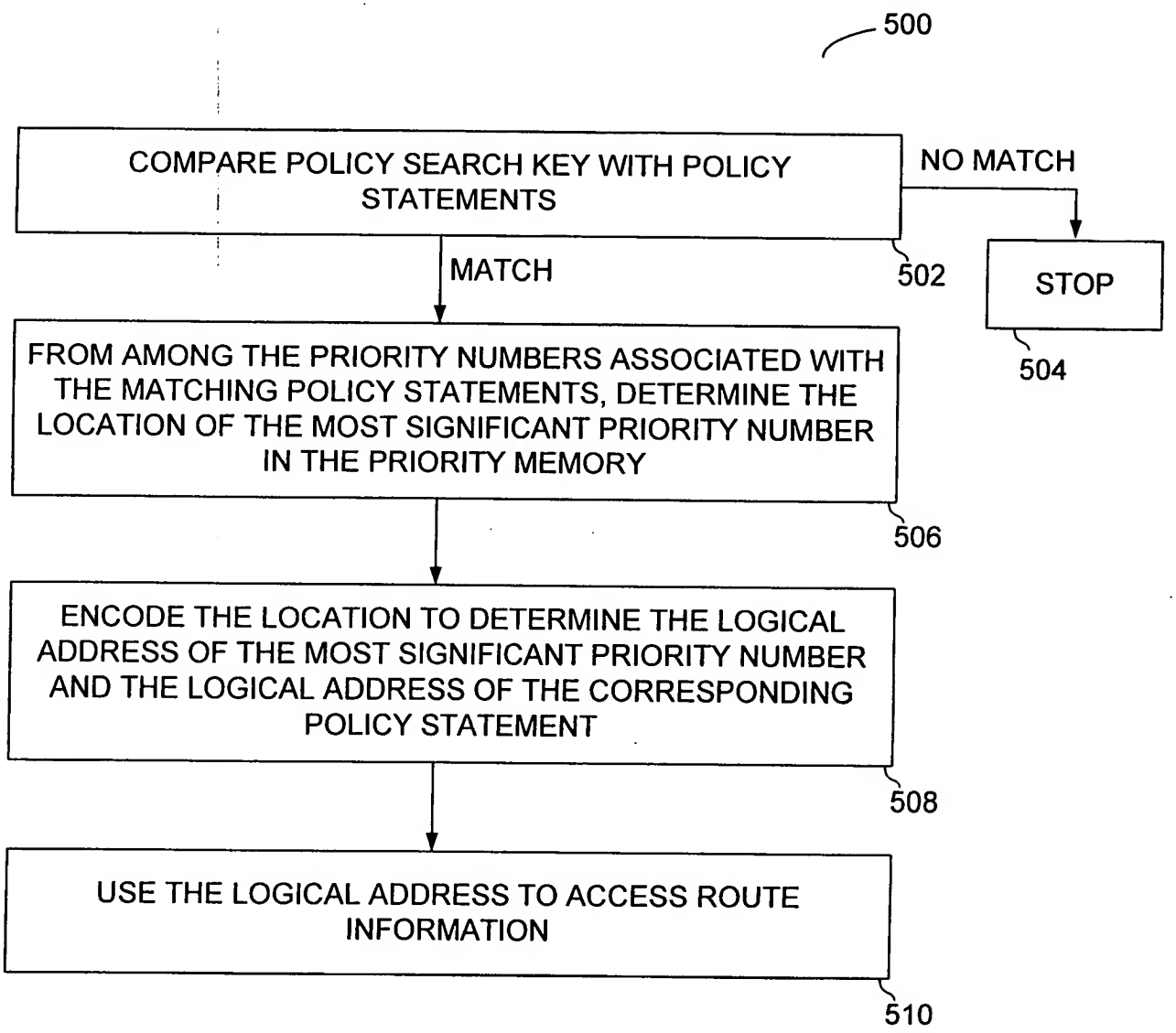

500
COMPARE POLICY SEARCH KEY WITH POLICY STATEMENTS
NO MATCH
MATCH
502
STOP
504
FROM AMONG THE PRIORITY NUMBERS ASSOCIATED WITH THE MATCHING POLICY STATEMENTS, DETERMINE THE LOCATION OF THE MOST SIGNIFICANT PRIORITY NUMBER IN THE PRIORITY MEMORY
506
ENCODE THE LOCATION TO DETERMINE THE LOGICAL ADDRESS OF THE MOST SIGNIFICANT PRIORITY NUMBER AND THE LOGICAL ADDRESS OF THE CORRESPONDING POLICY STATEMENT
508
USE THE LOGICAL ADDRESS TO ACCESS ROUTE INFORMATION
510

FIG. 5

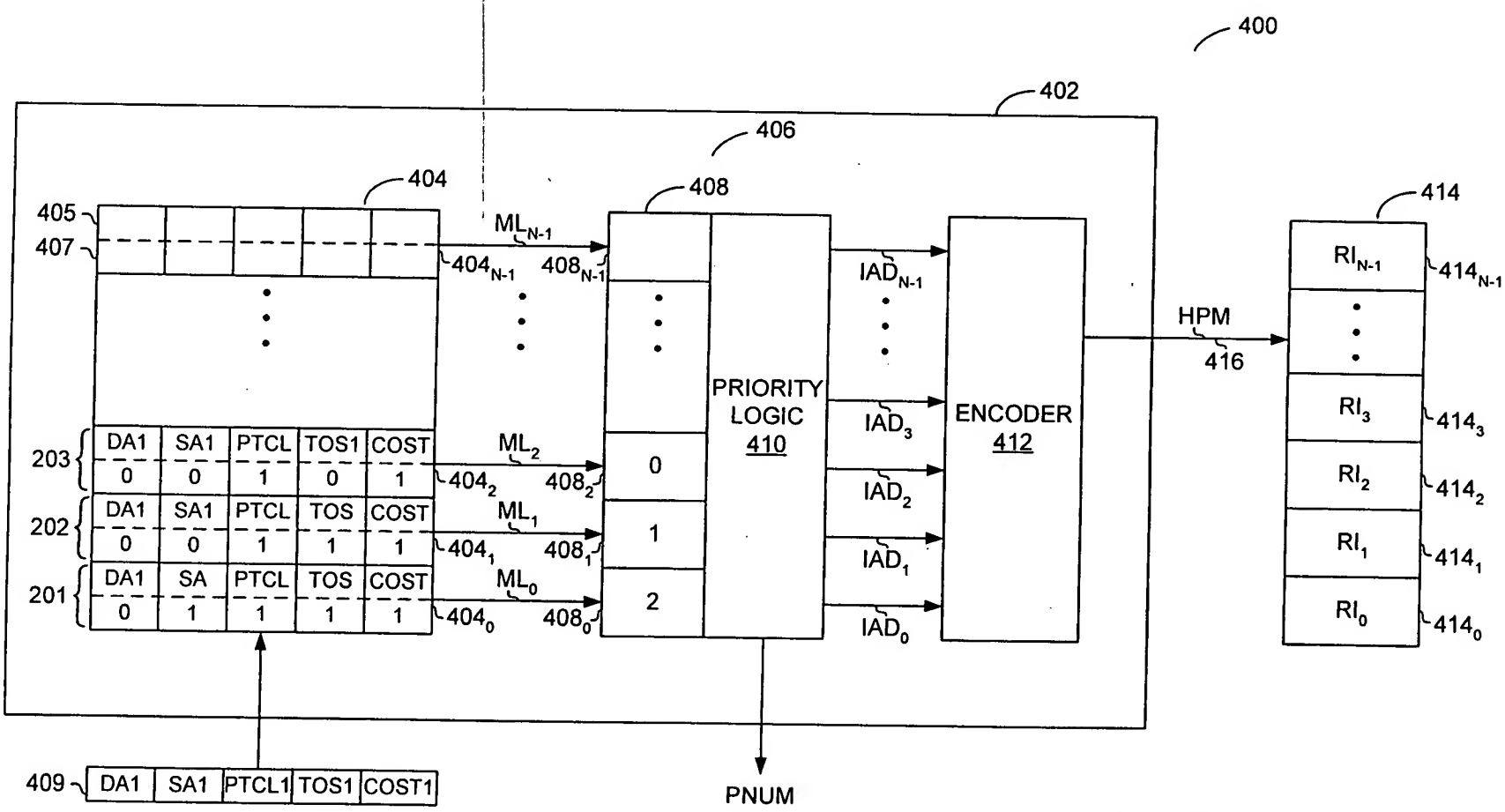

400
402
406
404
408
414
405
407
ML_{N-1}
404_{N-1}
408_{N-1}
IAD_{N-1}
RI_{N-1}
414_{N-1}
PRIORITY LOGIC 410
ENCODER 412
HPM
416
203
DA1 SA1 PTCL TOS1 COST
0 0 1 0 1
ML_2
404_2
408_2
0
IAD_3
RI_3
414_3
202
DA1 SA1 PTCL TOS COST
0 0 1 1 1
ML_1
404_1
408_1
1
IAD_2
RI_2
414_2
201
DA1 SA PTCL TOS COST
0 1 1 1 1
ML_0
404_0
408_0
2
IAD_1
RI_1
414_1
IAD_0
RI_0
414_0
409
DA1 SA1 PTCL1 TOS1 COST1
PNUM

FIG. 6

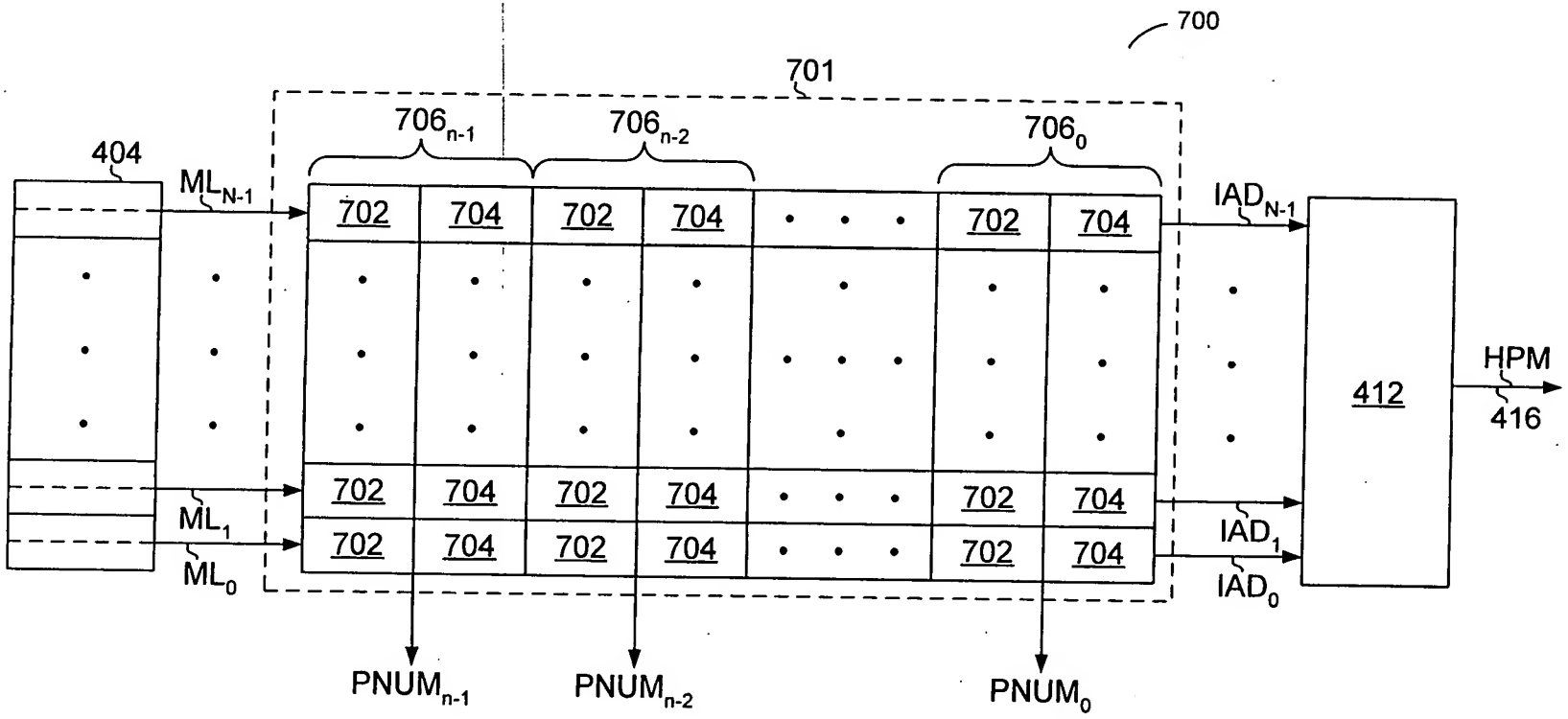

700
701
404
706_{n-1}
706_{n-2}
706_0
ML_{N-1}
ML_1
ML_0
702
704
IAD_{N-1}
IAD_1
IAD_0
412
HPM
416
$PNUM_{n-1}$
$PNUM_{n-2}$
$PNUM_0$

FIG. 7

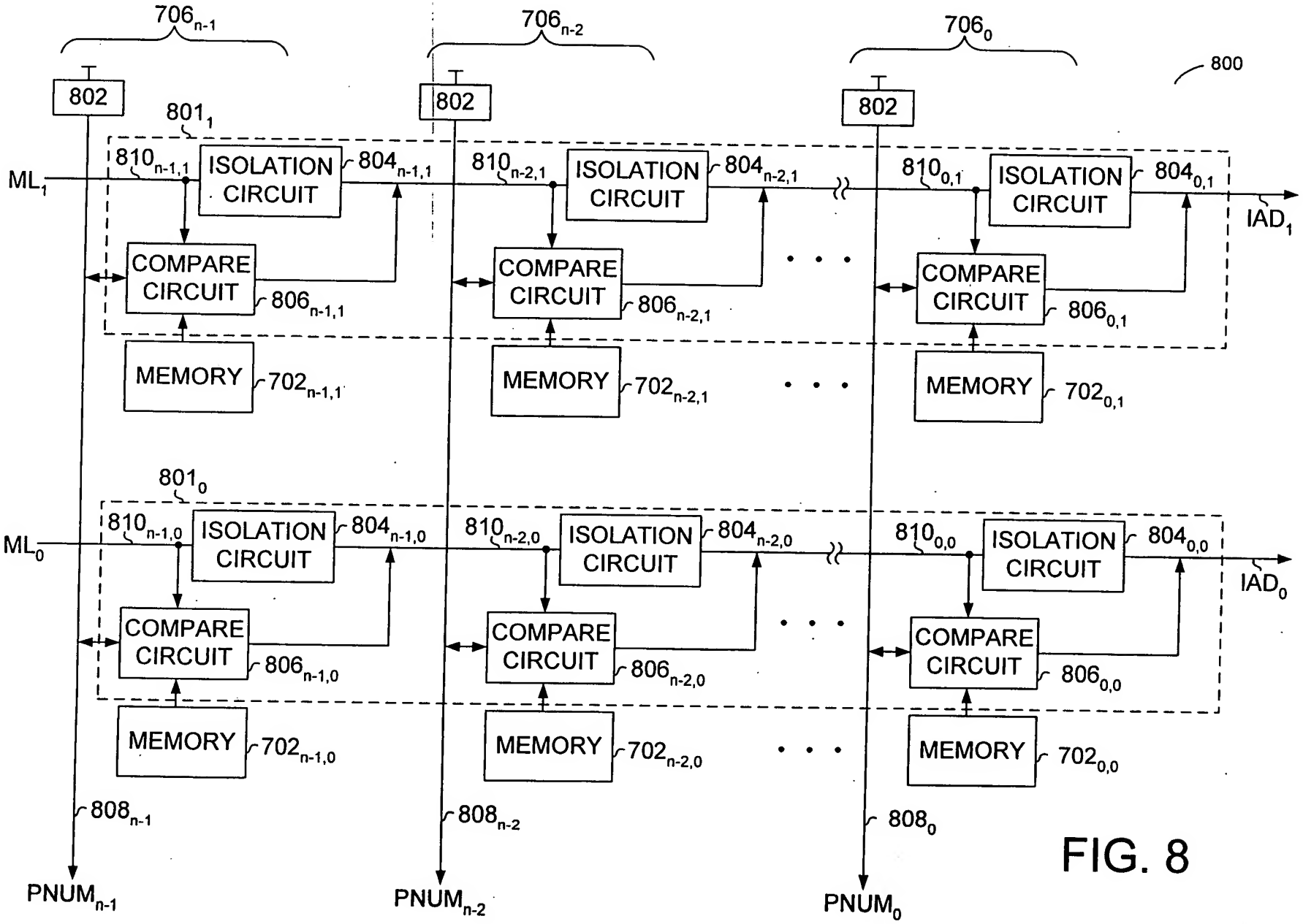

706n-1
706n-2
706o
800
802
802
802
801 1
801 0
ML1
ML0
810n-1,1
ISOLATION CIRCUIT
804n-1,1
810n-2,1
ISOLATION CIRCUIT
804n-2,1
810o,1
ISOLATION CIRCUIT
804o,1
IAD1
COMPARE CIRCUIT
806n-1,1
COMPARE CIRCUIT
806n-2,1
COMPARE CIRCUIT
806o,1
MEMORY
702n-1,1
MEMORY
702n-2,1
MEMORY
702o,1
810n-1,0
ISOLATION CIRCUIT
804n-1,0
810n-2,0
ISOLATION CIRCUIT
804n-2,0
810o,0
ISOLATION CIRCUIT
804o,0
IAD0
COMPARE CIRCUIT
806n-1,0
COMPARE CIRCUIT
806n-2,0
COMPARE CIRCUIT
806o,0
MEMORY
702n-1,0
MEMORY
702n-2,0
MEMORY
702o,0
808n-1
808n-2
808o
PNUMn-1
PNUMn-2
PNUMo

FIG. 8

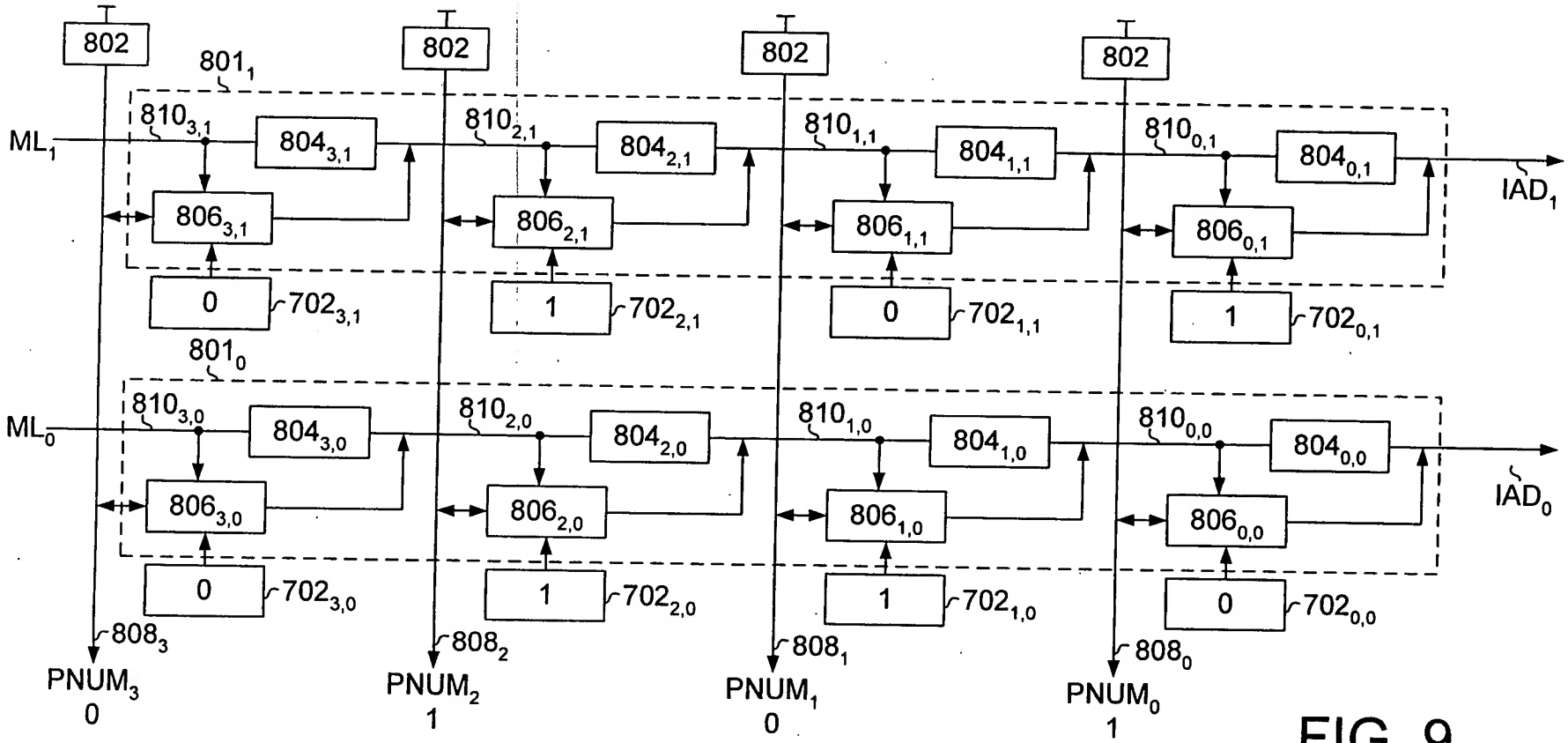

802
801$_1$
810$_{3,1}$
804$_{3,1}$
806$_{3,1}$
0
702$_{3,1}$
810$_{2,1}$
804$_{2,1}$
806$_{2,1}$
1
702$_{2,1}$
810$_{1,1}$
804$_{1,1}$
806$_{1,1}$
0
702$_{1,1}$
810$_{0,1}$
804$_{0,1}$
806$_{0,1}$
1
702$_{0,1}$
ML$_1$
IAD$_1$
801$_0$
810$_{3,0}$
804$_{3,0}$
806$_{3,0}$
0
702$_{3,0}$
810$_{2,0}$
804$_{2,0}$
806$_{2,0}$
1
702$_{2,0}$
810$_{1,0}$
804$_{1,0}$
806$_{1,0}$
1
702$_{1,0}$
810$_{0,0}$
804$_{0,0}$
806$_{0,0}$
0
702$_{0,0}$
ML$_0$
IAD$_0$
808$_3$
PNUM$_3$
0
808$_2$
PNUM$_2$
1
808$_1$
PNUM$_1$
0
808$_0$
PNUM$_0$
1

FIG. 9

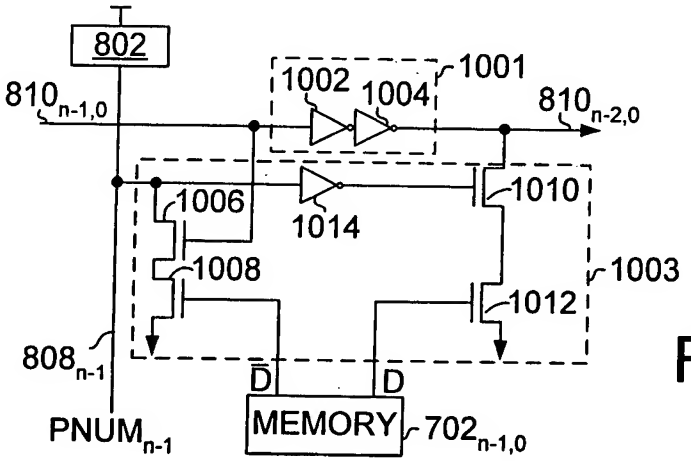

802
810$_{n-1,0}$
1002
1004
1001
810$_{n-2,0}$
1006
1014
1010
1008
1003
1012
808$_{n-1}$
D
D
PNUM$_{n-1}$
MEMORY
702$_{n-1,0}$

FIG. 10

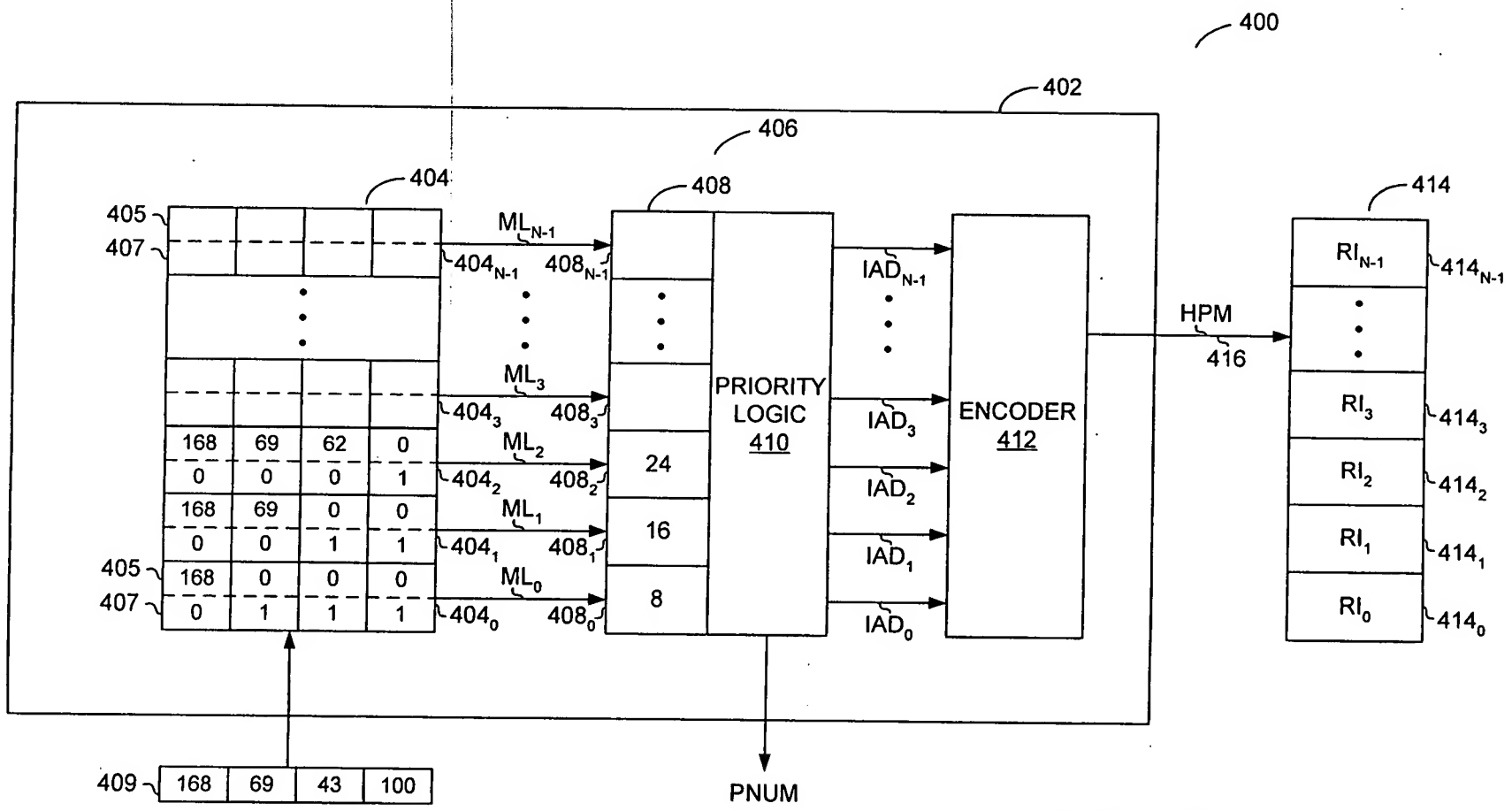

400
402
406
404
408
414
405
407
ML_{N-1}
404_{N-1}
408_{N-1}
ML_3
404_3
408_3
ML_2
404_2
408_2
ML_1
404_1
408_1
ML_0
404_0
408_0
168 69 62 0
0 0 0 1
168 69 0 0
0 0 1 1
168 0 0 0
0 1 1 1
24
16
8
PRIORITY LOGIC 410
IAD_{N-1}
IAD_3
IAD_2
IAD_1
IAD_0
ENCODER 412
HPM 416
RI_{N-1}
RI_3
RI_2
RI_1
RI_0
414_{N-1}
414_3
414_2
414_1
414_0
409
168 69 43 100
PNUM

FIG. 11

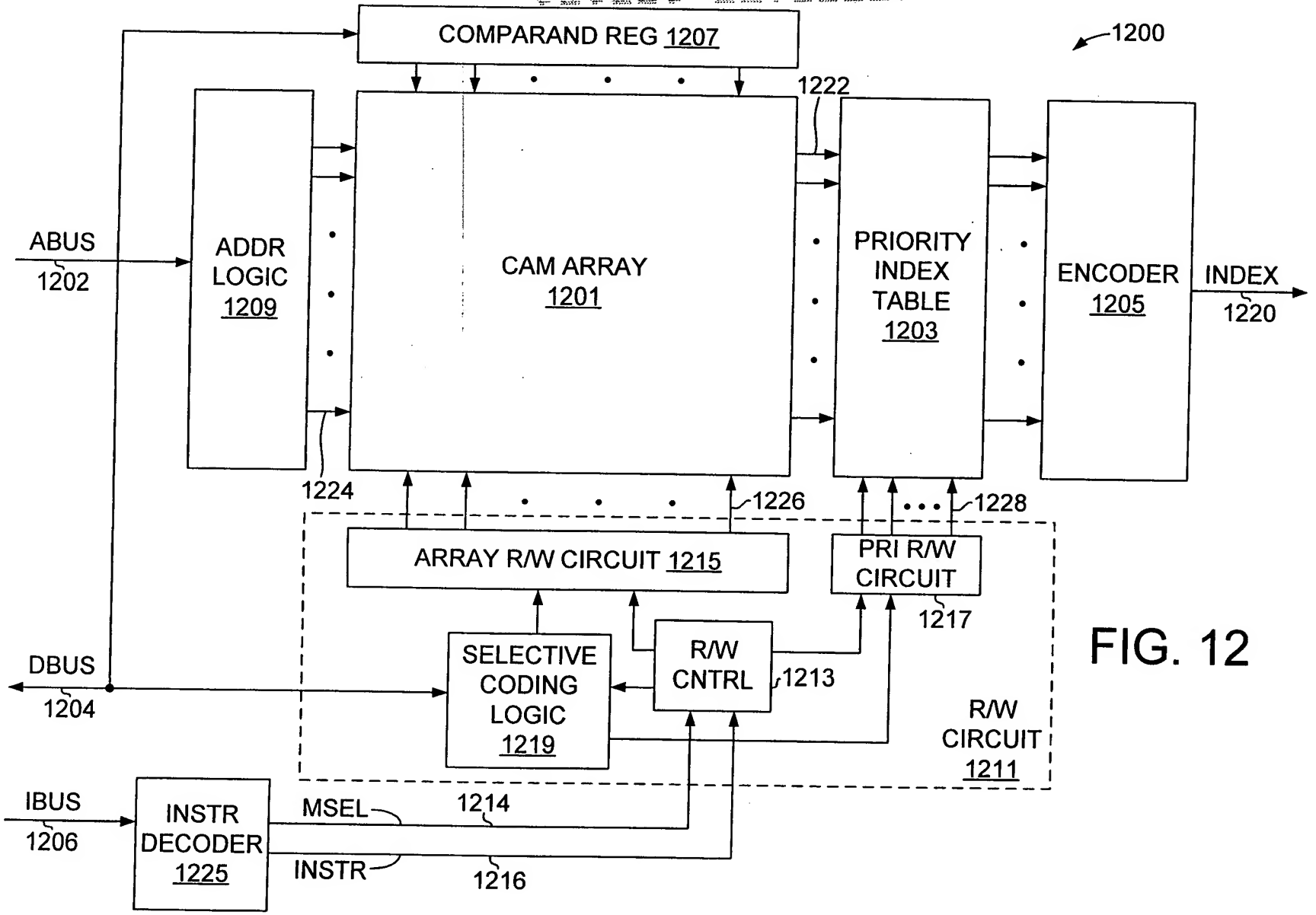

COMPARAND REG 1207
1200
1222
ABUS
1202
ADDR
LOGIC
1209
CAM ARRAY
1201
PRIORITY
INDEX
TABLE
1203
ENCODER
1205
INDEX
1220
1224
1226
1228
ARRAY R/W CIRCUIT 1215
PRI R/W
CIRCUIT
1217
DBUS
1204
SELECTIVE
CODING
LOGIC
1219
R/W
CNTRL
1213
R/W
CIRCUIT
1211
IBUS
1206
INSTR
DECODER
1225
MSEL
1214
INSTR
1216

FIG. 12

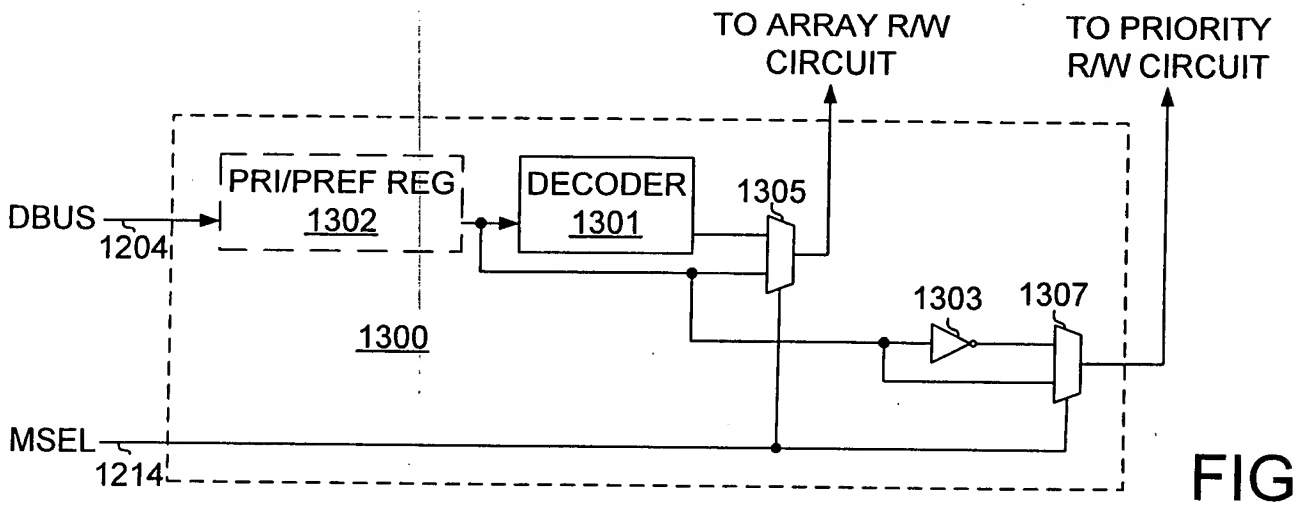

TO ARRAY R/W CIRCUIT
TO PRIORITY R/W CIRCUIT
PRI/PREF REG 1302
DECODER 1301
1305
DBUS 1204
1303
1307
1300
MSEL 1214

FIG. 13

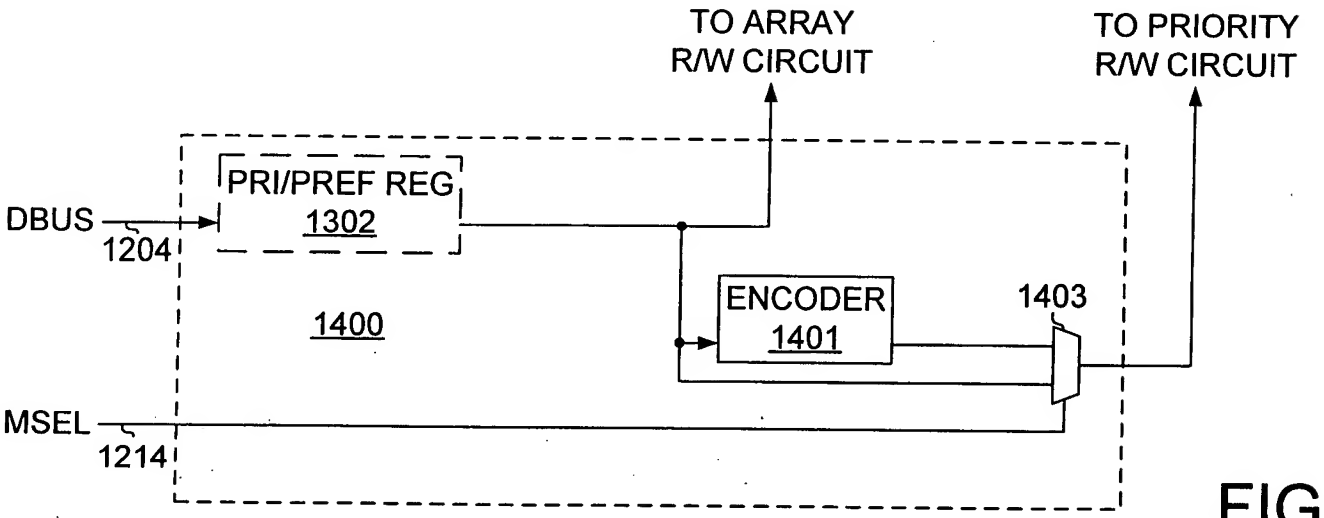

TO ARRAY R/W CIRCUIT
TO PRIORITY R/W CIRCUIT
PRI/PREF REG 1302
DBUS 1204
ENCODER 1401
1403
1400
MSEL 1214

FIG. 14

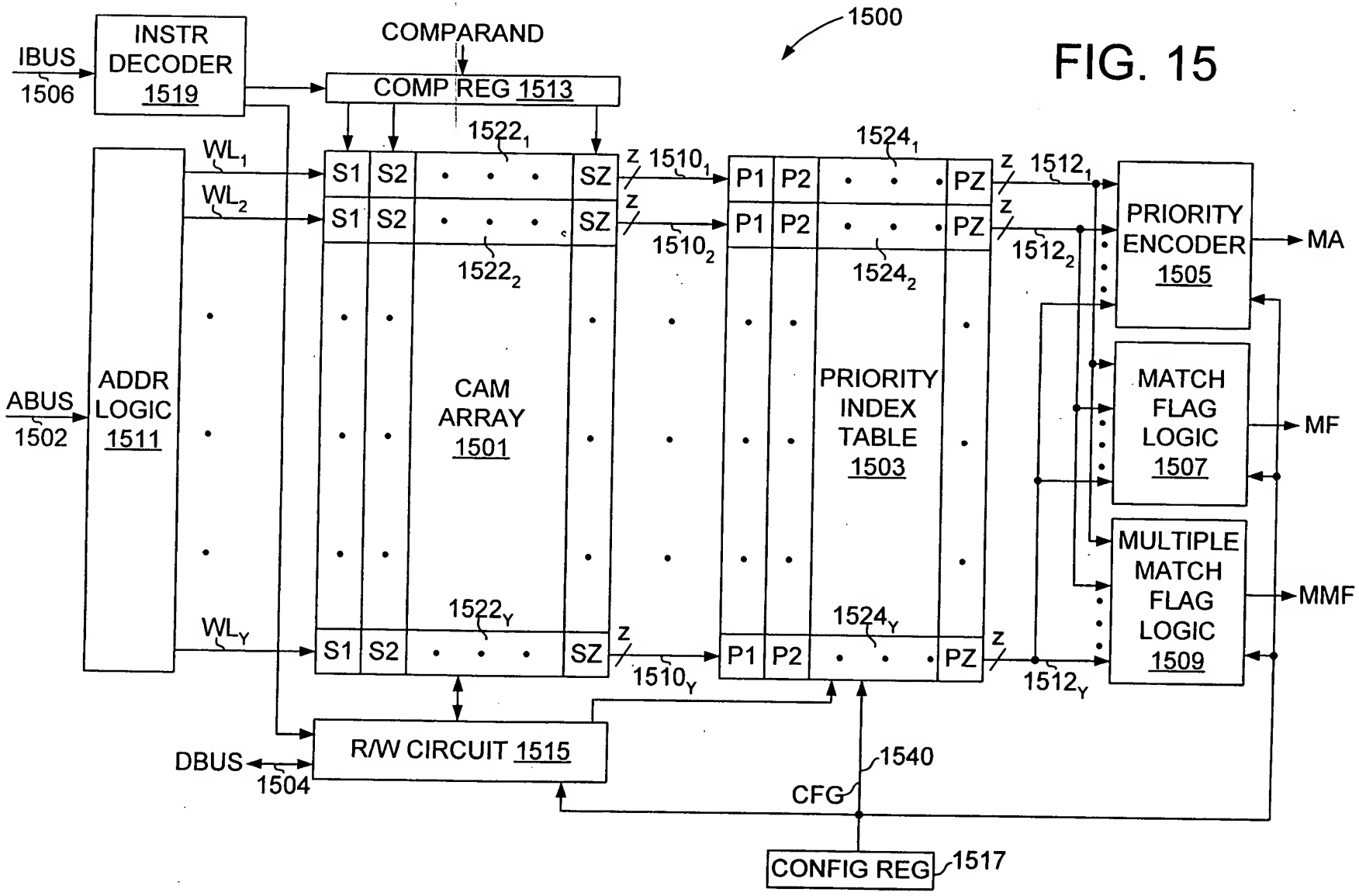

1500
INSTR DECODER 1519
IBUS 1506
COMPARAND
COMP REG 1513
ADDR LOGIC 1511
ABUS 1502
CAM ARRAY 1501
PRIORITY INDEX TABLE 1503
PRIORITY ENCODER 1505
MATCH FLAG LOGIC 1507
MULTIPLE MATCH FLAG LOGIC 1509
MA
MF
MMF
R/W CIRCUIT 1515
DBUS 1504
CFG 1540
CONFIG REG 1517
WL1
WL2
WLY
S1
S2
SZ
P1
P2
PZ
1522_1
1522_2
1522_Y
1524_1
1524_2
1524_Y
1510_1
1510_2
1510_Y
1512_1
1512_2
1512_Y
Z

FIG. 15

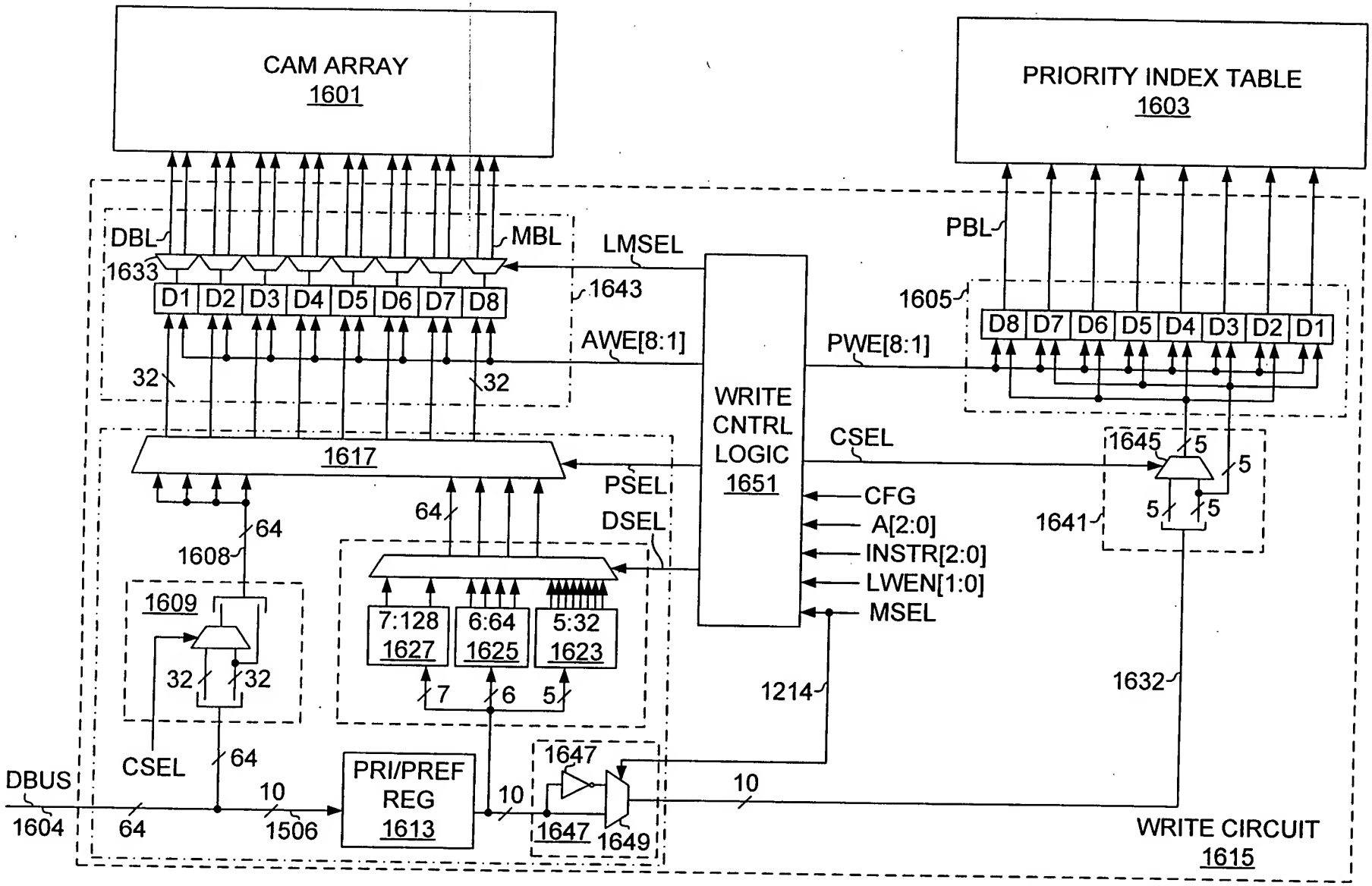

CAM ARRAY
1601
PRIORITY INDEX TABLE
1603
DBL
MBL
LMSEL
1633
1643
PBL
1605
D1 D2 D3 D4 D5 D6 D7 D8
D8 D7 D6 D5 D4 D3 D2 D1
AWE[8:1]
PWE[8:1]
32
32
WRITE
CNTRL
LOGIC
1651
1617
PSEL
CSEL
1645
5
5
CFG
A[2:0]
INSTR[2:0]
LWEN[1:0]
MSEL
64
64
DSEL
1608
1641
5
5
1609
7:128
1627
6:64
1625
5:32
1623
32
32
7
6
5
1214
1632
CSEL
64
1647
DBUS
10
PRI/PREF
REG
1613
10
10
1604
64
1506
1647
1649
WRITE CIRCUIT
1615

FIG. 16

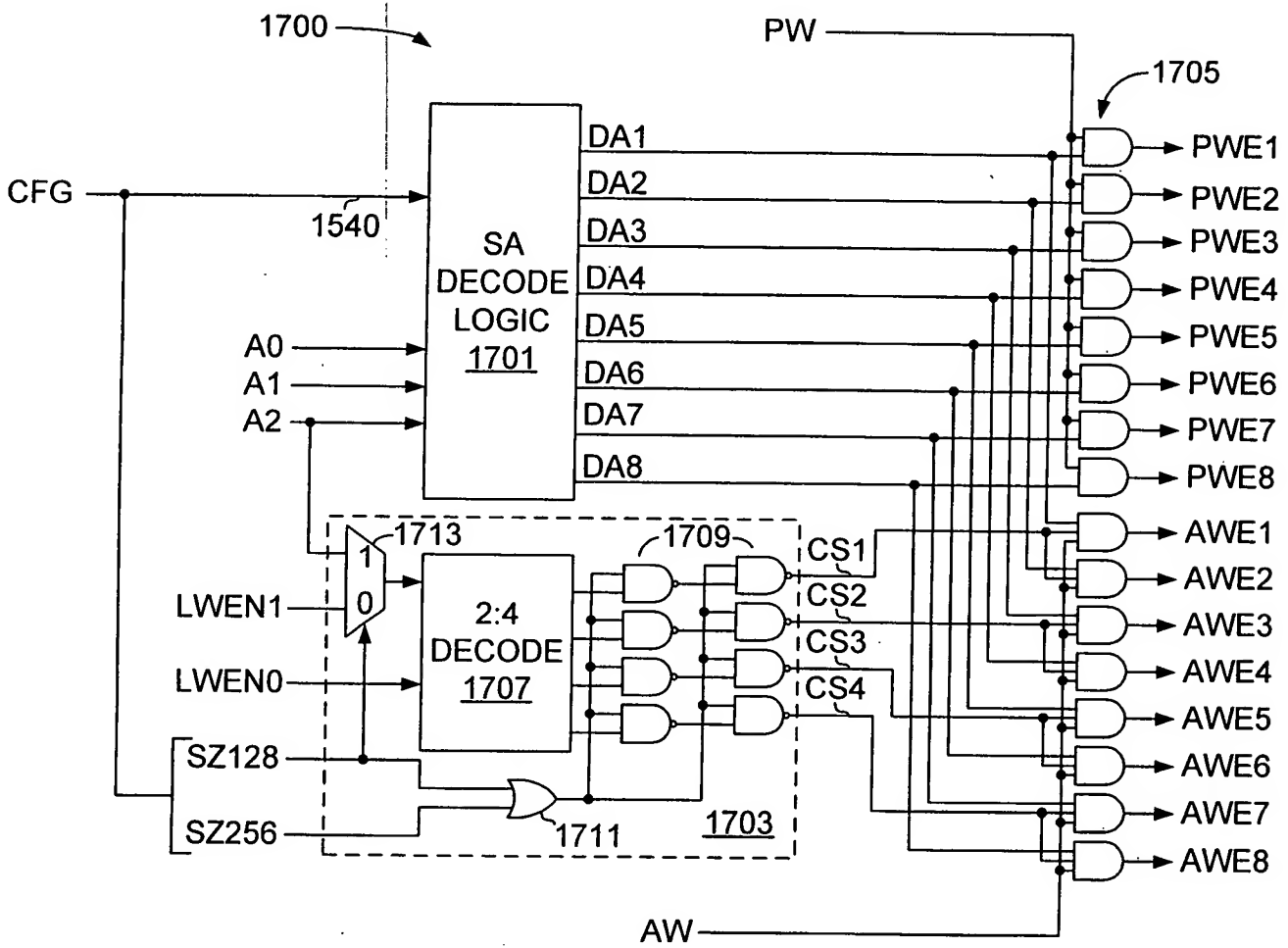
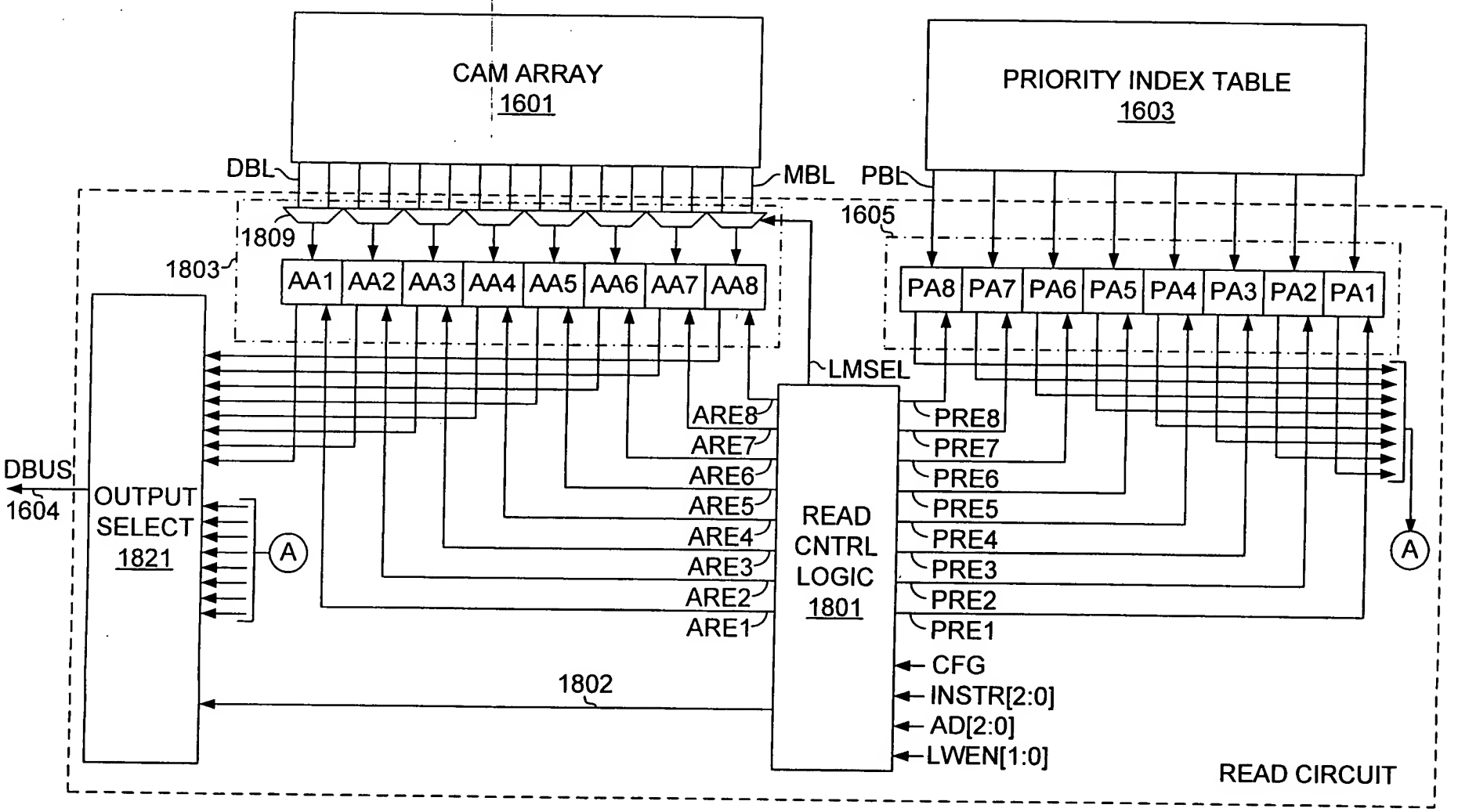

1700
PW
1705
CFG
1540
SA
DECODE
LOGIC
1701
DA1
DA2
DA3
DA4
DA5
DA6
DA7
DA8
A0
A1
A2
PWE1
PWE2
PWE3
PWE4
PWE5
PWE6
PWE7
PWE8
1713
1709
1
0
LWEN1
LWEN0
2:4
DECODE
1707
CS1
CS2
CS3
CS4
AWE1
AWE2
AWE3
AWE4
AWE5
AWE6
AWE7
AWE8
SZ128
SZ256
1711
1703
AW

FIG. 17

FIG. 18


CAM ARRAY
1601
PRIORITY INDEX TABLE
1603
DBL
MBL
PBL
1605
1809
1803
AA1
AA2
AA3
AA4
AA5
AA6
AA7
AA8
PA8
PA7
PA6
PA5
PA4
PA3
PA2
PA1
LMSEL
ARE8
ARE7
ARE6
ARE5
ARE4
ARE3
ARE2
ARE1
PRE8
PRE7
PRE6
PRE5
PRE4
PRE3
PRE2
PRE1
DBUS
1604
OUTPUT
SELECT
1821
A
READ
CNTRL
LOGIC
1801
CFG
INSTR[2:0]
AD[2:0]
LWEN[1:0]
1802
READ CIRCUIT

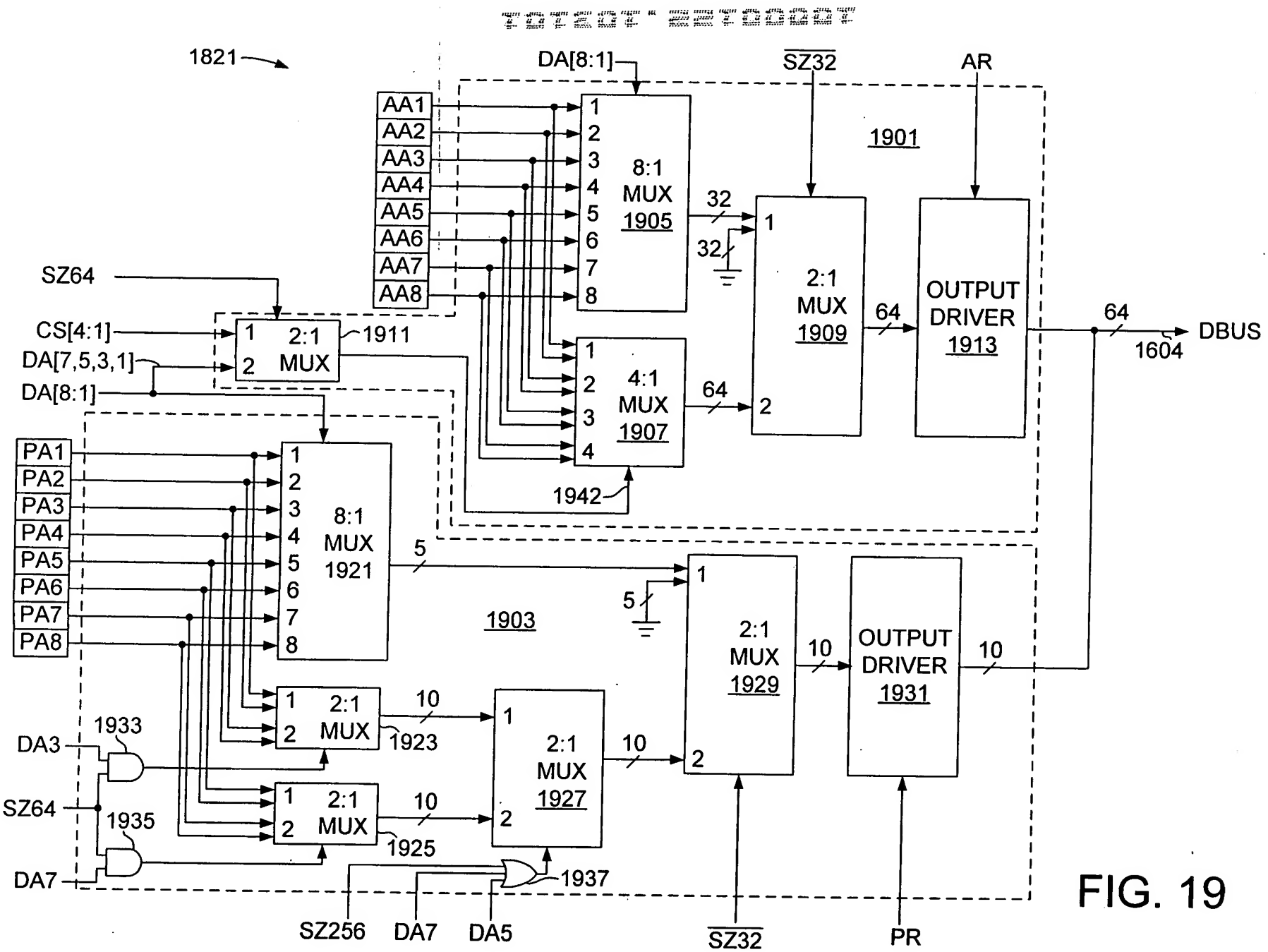

1821
DA[8:1]
SZ32
AR
AA1
AA2
AA3
AA4
AA5
AA6
AA7
AA8
8:1 MUX 1905
1901
32
32
2:1 MUX 1909
64
OUTPUT DRIVER 1913
64
1604
DBUS
SZ64
CS[4:1]
DA[7,5,3,1]
DA[8:1]
2:1 MUX
1911
4:1 MUX 1907
64
1942
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PA8
8:1 MUX 1921
5
1903
5
2:1 MUX 1929
10
OUTPUT DRIVER 1931
10
2:1 MUX
1923
10
1933
DA3
2:1 MUX 1927
10
SZ64
1935
2:1 MUX
1925
10
DA7
1937
SZ256
DA7
DA5
SZ32
PR

FIG. 19

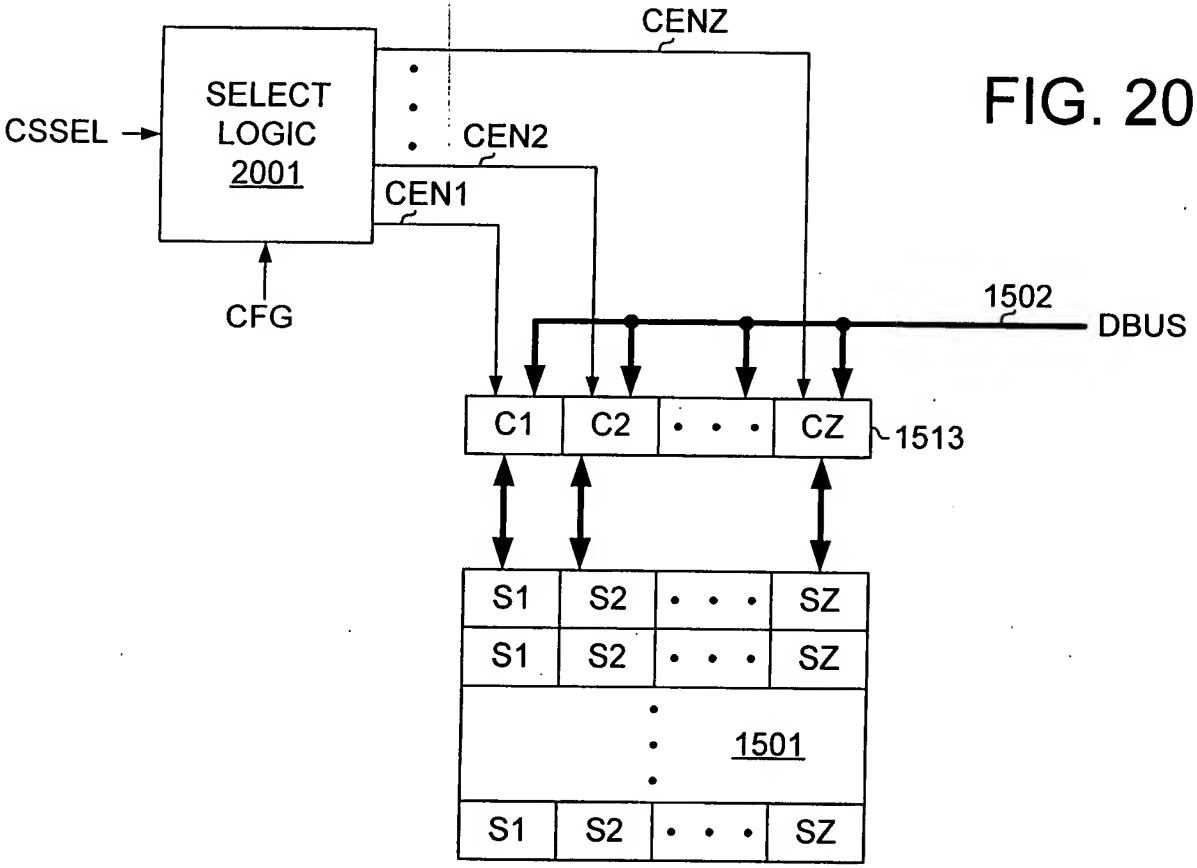

CENZ
SELECT
LOGIC
2001
CSSEL
CEN2
CEN1
CFG
1502
DBUS
C1
C2
CZ
1513
S1
S2
SZ
1501

FIG. 20

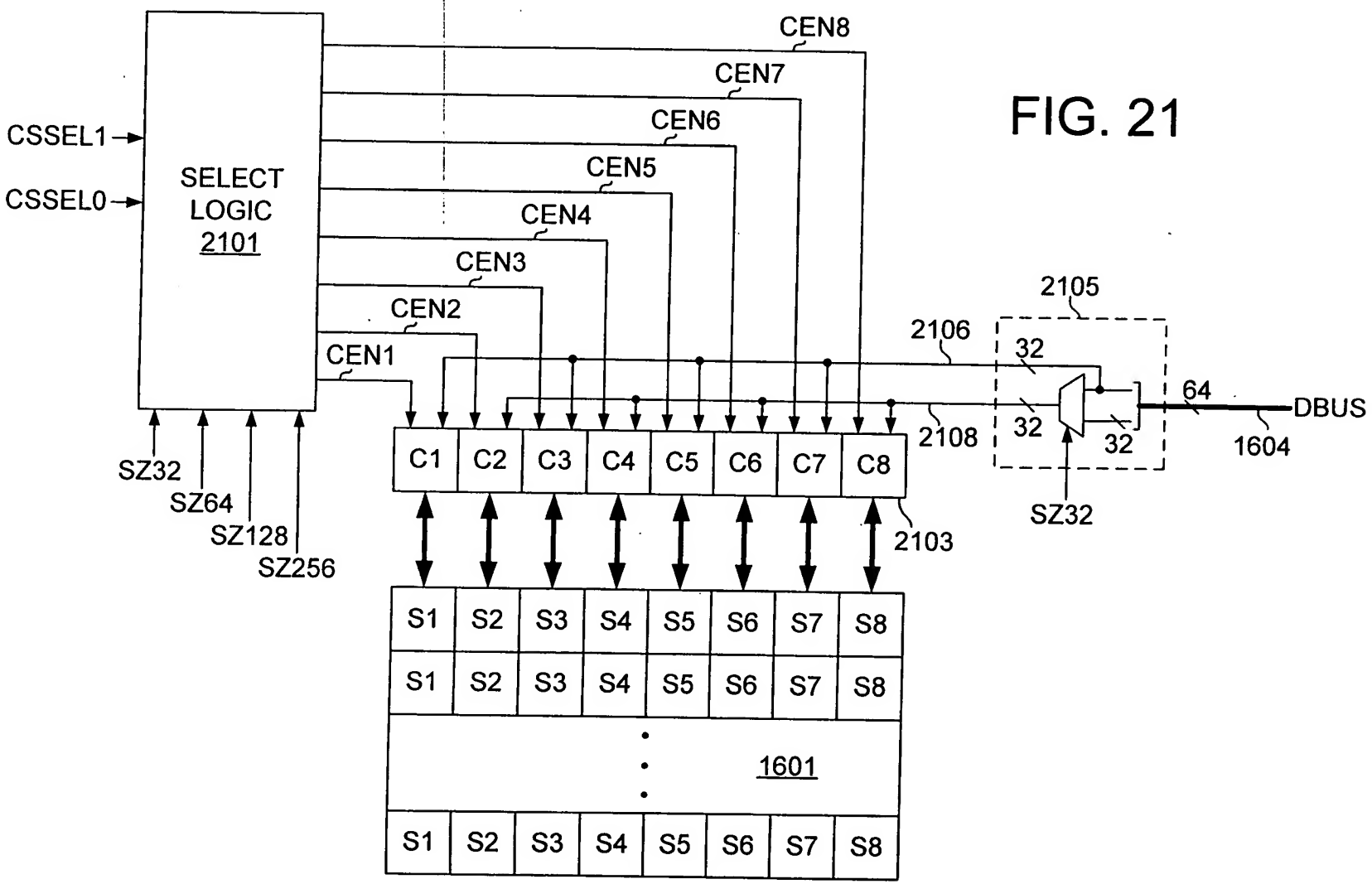

CSSEL1
CSSEL0
SELECT LOGIC 2101
CEN8
CEN7
CEN6
CEN5
CEN4
CEN3
CEN2
CEN1
SZ32
SZ64
SZ128
SZ256
C1 C2 C3 C4 C5 C6 C7 C8
2103
2105
2106
2108
32
32
32
64
DBUS
1604
SZ32
S1 S2 S3 S4 S5 S6 S7 S8
S1 S2 S3 S4 S5 S6 S7 S8
1601
S1 S2 S3 S4 S5 S6 S7 S8

FIG. 21

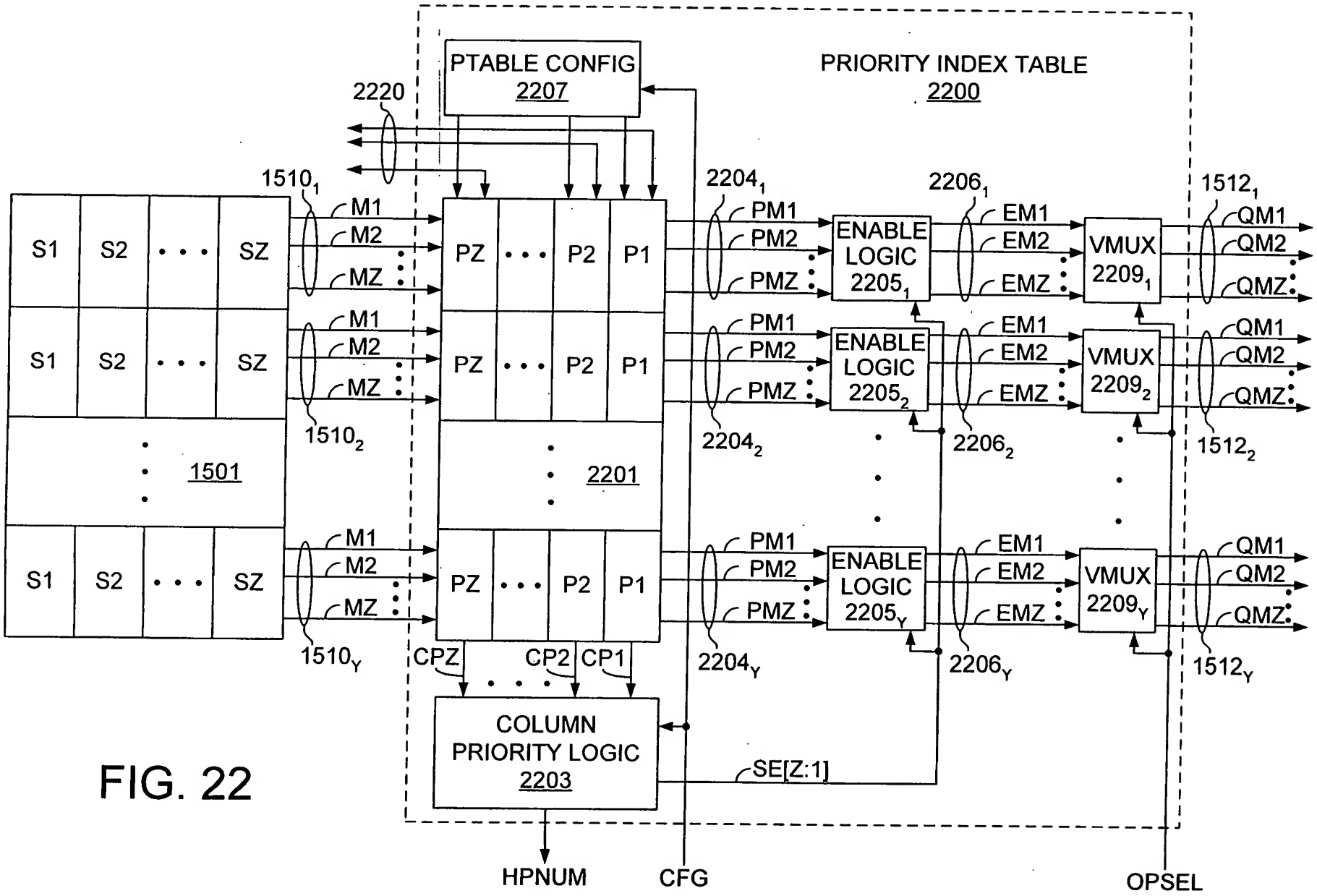

PTABLE CONFIG
2207
PRIORITY INDEX TABLE
2200
2220
1510$_1$
1510$_2$
1510$_Y$
S1
S2
SZ
1501
M1
M2
MZ
PZ
P2
P1
2201
2204$_1$
2204$_2$
2204$_Y$
PM1
PM2
PMZ
ENABLE LOGIC 2205$_1$
ENABLE LOGIC 2205$_2$
ENABLE LOGIC 2205$_Y$
2206$_1$
2206$_2$
2206$_Y$
EM1
EM2
EMZ
VMUX 2209$_1$
VMUX 2209$_2$
VMUX 2209$_Y$
1512$_1$
1512$_2$
1512$_Y$
QM1
QM2
QMZ
CPZ
CP2
CP1
COLUMN PRIORITY LOGIC 2203
SE[Z:1]
HPNUM
CFG
OPSEL

FIG. 22

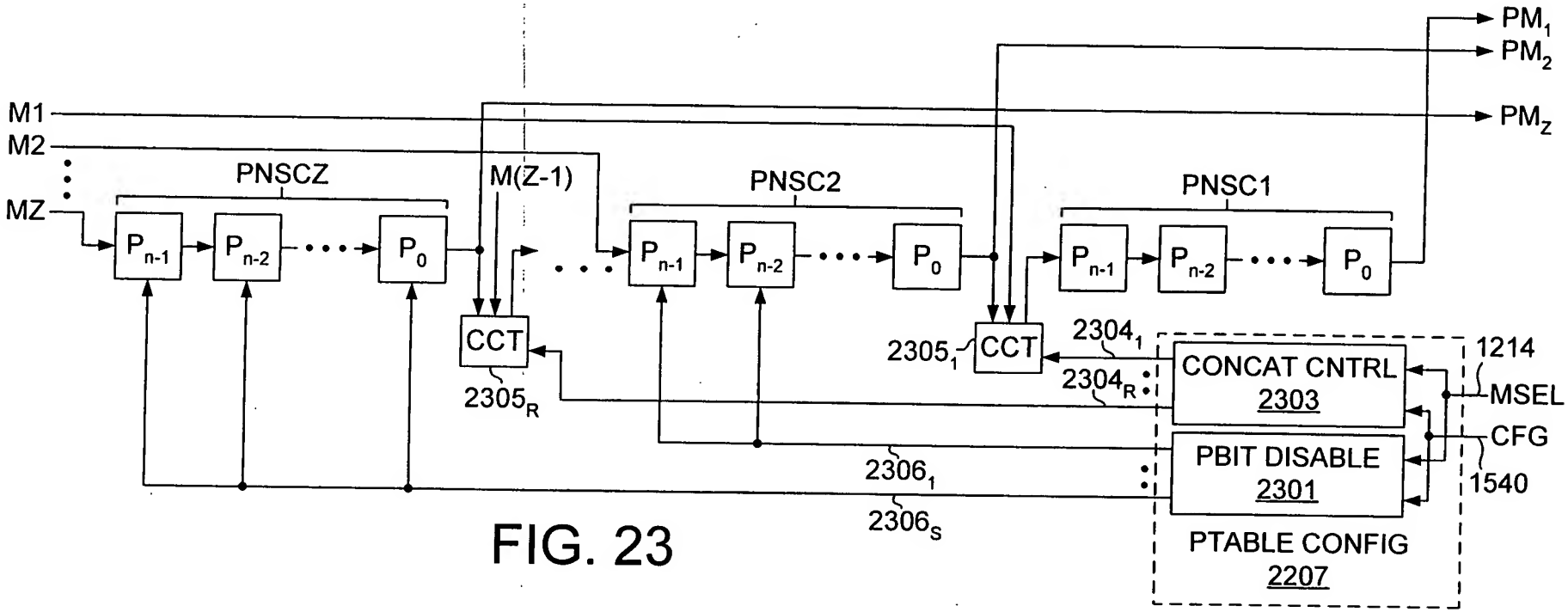


FIG. 23

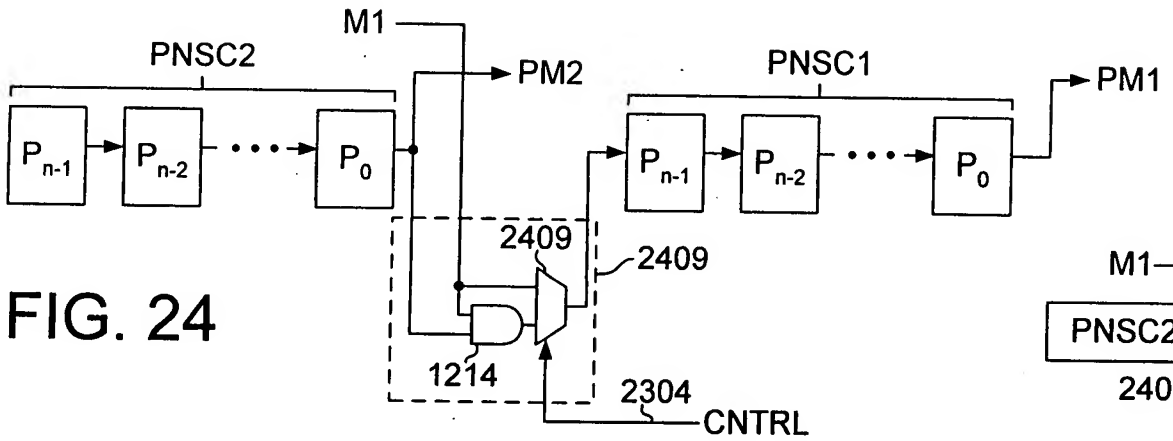


FIG. 24

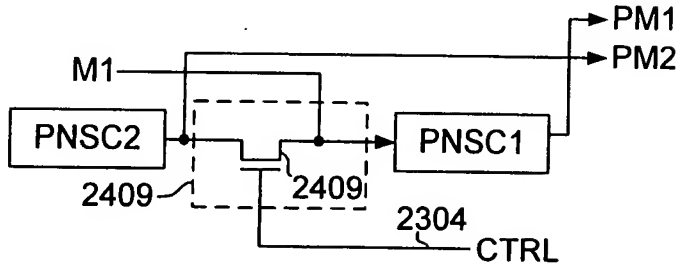


FIG. 25

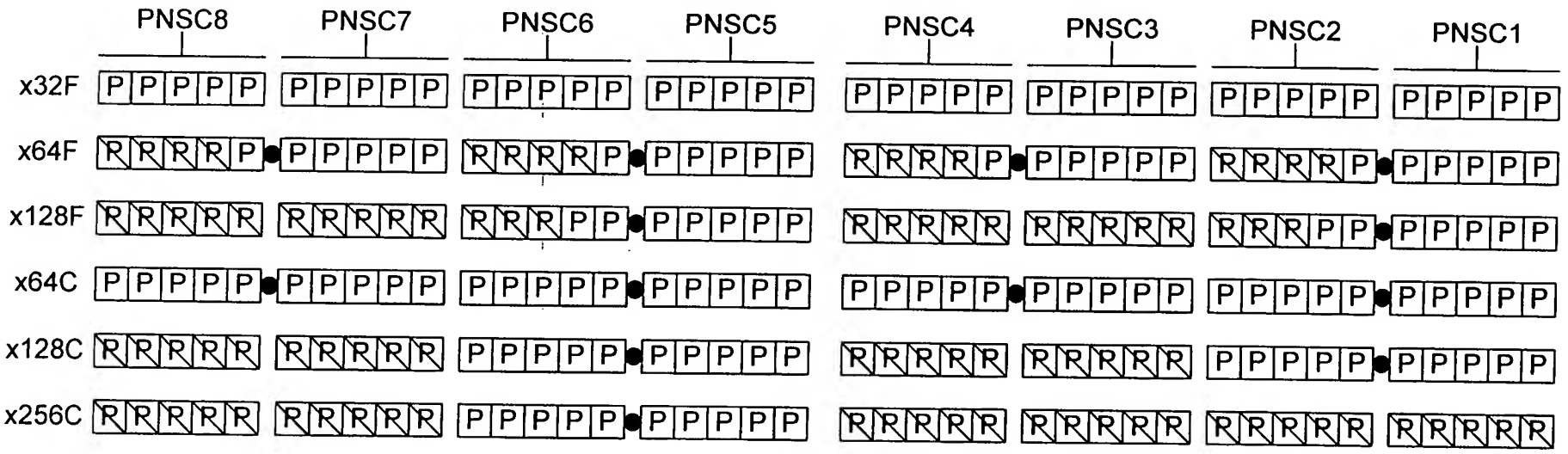

PNSC8
PNSC7
PNSC6
PNSC5
PNSC4
PNSC3
PNSC2
PNSC1
x32F
x64F
x128F
x64C
x128C
x256C

FIG. 26

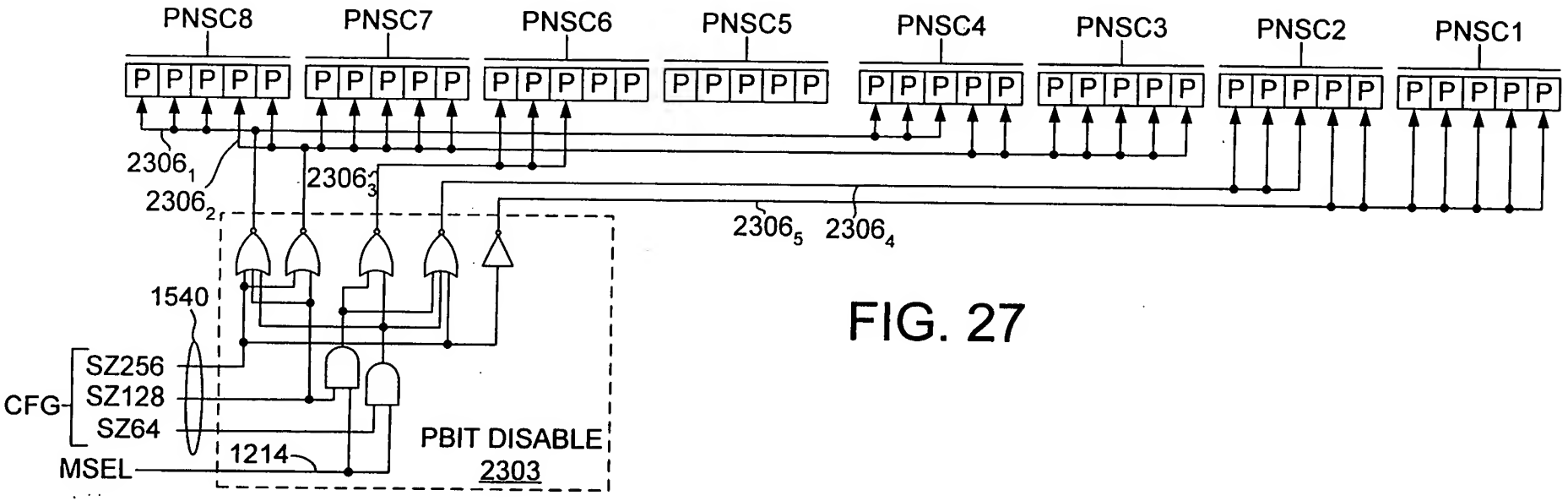

PNSC8
PNSC7
PNSC6
PNSC5
PNSC4
PNSC3
PNSC2
PNSC1
2306₁
2306₂
2306₃
2306₅
2306₄
1540
SZ256
SZ128
SZ64
CFG
MSEL
1214
PBIT DISABLE
2303

FIG. 27

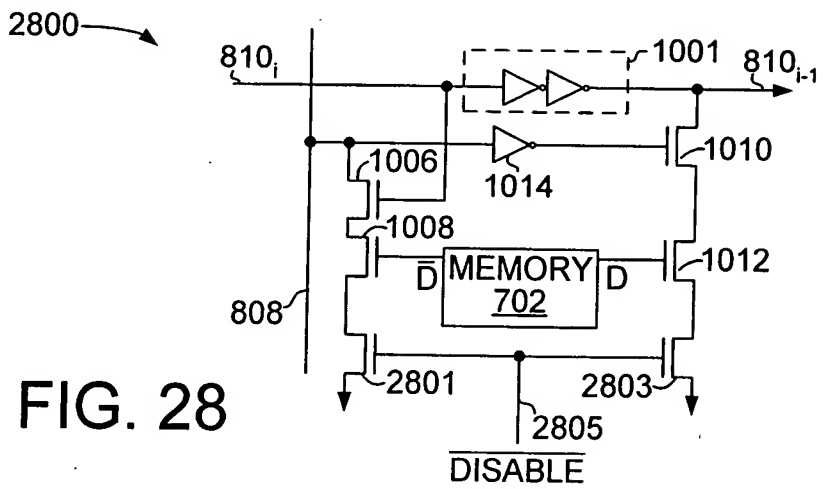

2800
810i
1001
810i-1
1006
1014
1010
1008
MEMORY
702
D
D
1012
808
2801
2803
2805
DISABLE

FIG. 28

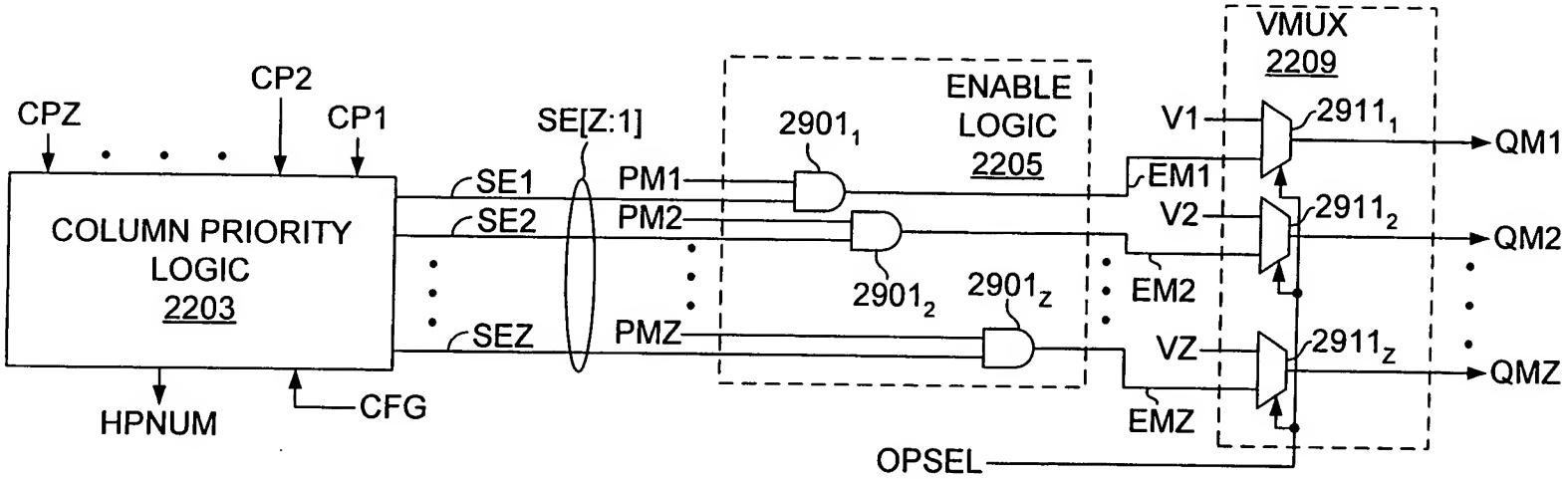

CPZ
CP2
CP1
SE[Z:1]
COLUMN PRIORITY LOGIC 2203
SE1
SE2
SEZ
HPNUM
CFG
PM1
PM2
PMZ
2901₁
2901₂
2901z
ENABLE LOGIC 2205
EM1
EM2
EMZ
VMUX 2209
V1
V2
VZ
2911₁
2911₂
2911z
QM1
QM2
QMZ
OPSEL

FIG. 29

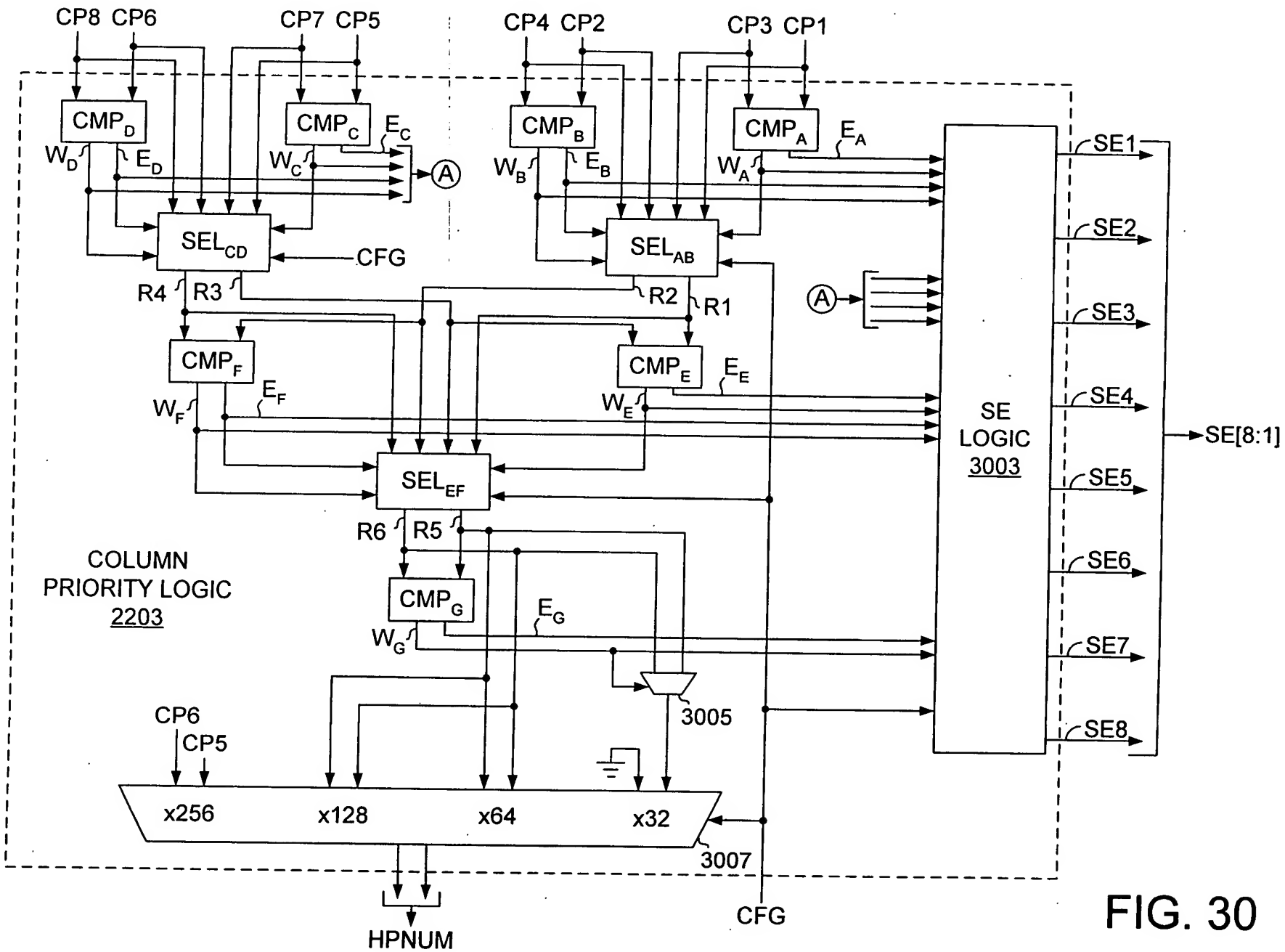

CP8 CP6
CP7 CP5
CP4 CP2
CP3 CP1
CMP_D
CMP_C
CMP_B
CMP_A
W_D
E_D
W_C
E_C
W_B
E_B
W_A
E_A
A
SEL_CD
SEL_AB
CFG
R4
R3
R2
R1
CMP_F
CMP_E
W_F
E_F
W_E
E_E
SEL_EF
R6
R5
CMP_G
W_G
E_G
COLUMN
PRIORITY LOGIC
2203
3005
CP6
CP5
x256
x128
x64
x32
3007
HPNUM
CFG
SE
LOGIC
3003
SE1
SE2
SE3
SE4
SE5
SE6
SE7
SE8
SE[8:1]

FIG. 30

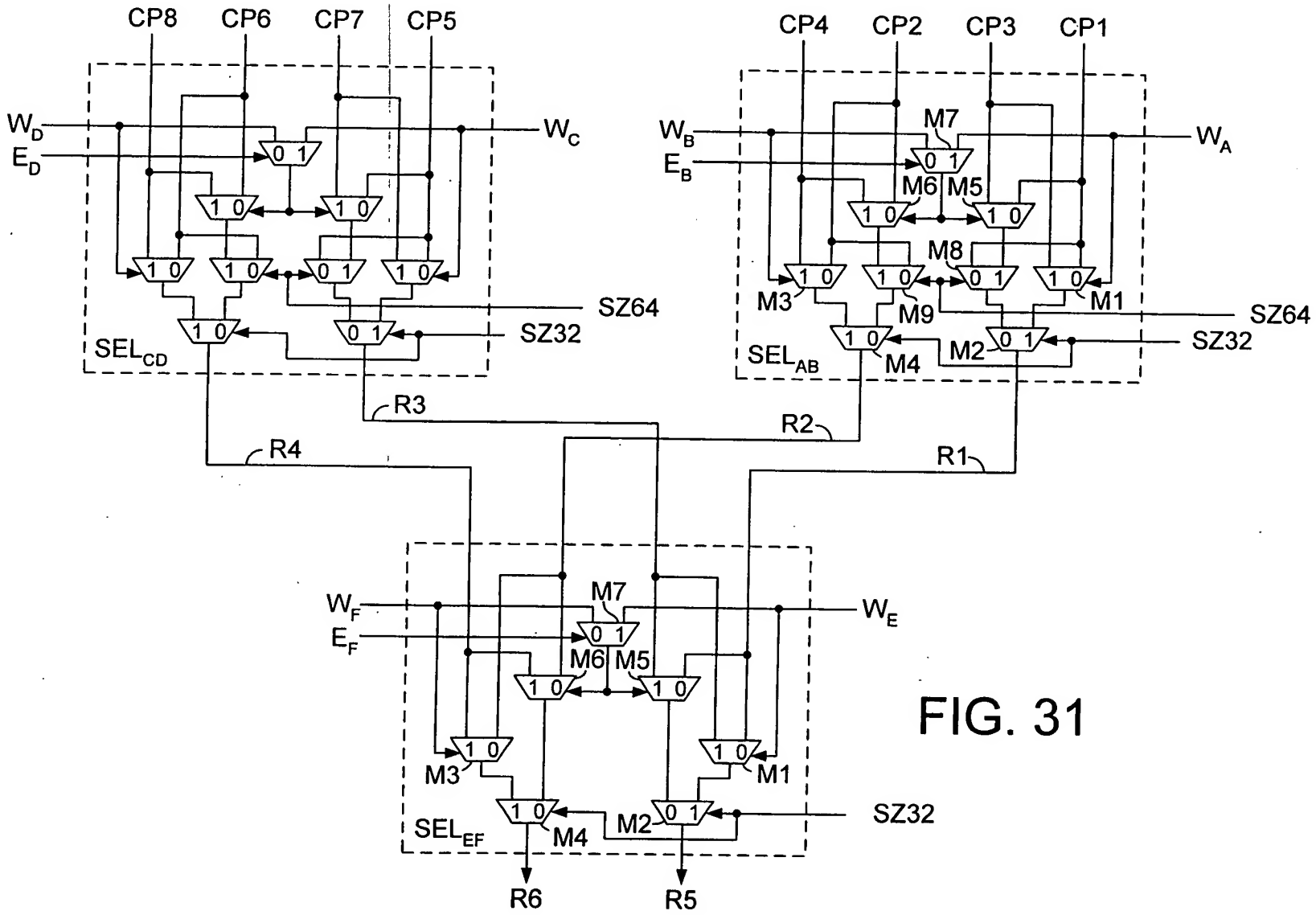

CP8
CP6
CP7
CP5
CP4
CP2
CP3
CP1
W_D
E_D
W_C
W_B
E_B
W_A
W_F
E_F
W_E
M7
M6
M5
M8
M9
M3
M1
M4
M2
SZ64
SZ32
SEL_{CD}
SEL_{AB}
SEL_{EF}
R1
R2
R3
R4
R5
R6

FIG. 31

FIG. 32

x64	x32	E_B	W_B	W_A	R2	R1
X	1	X	0	0	HP2	HP1
X	1	X	0	1	HP2	HP3
X	1	X	1	0	HP4	HP1
X	1	X	1	1	HP4	HP3
1	0	0	0	X	HP2	HP1
1	0	0	1	X	HP4	HP3
1	0	1	X	0	HP2	HP1
1	0	1	X	1	HP4	HP3
0	0	X	X	X	HP2	HP1

FIG. 33

x64	x32	E_D	W_D	W_C	R4	R3
X	1	X	0	0	HP6	HP5
X	1	X	0	1	HP6	HP7
X	1	X	1	0	HP8	HP5
X	1	X	1	1	HP8	HP7
1	0	0	0	X	HP6	HP5
1	0	0	1	X	HP8	HP7
1	0	1	X	0	HP6	HP5
1	0	1	X	1	HP8	HP7
0	0	X	X	X	HP6	HP5

FIG. 34

x32	E_F	W_F	W_E	R6	R5
1	X	0	0	R2	R1
1	X	0	1	R2	R3
1	X	1	0	R4	R1
1	X	1	1	R4	R3
0	0	0	X	R2	R1
0	0	1	X	R4	R3
0	1	X	0	R2	R1
0	1	X	1	R4	R3

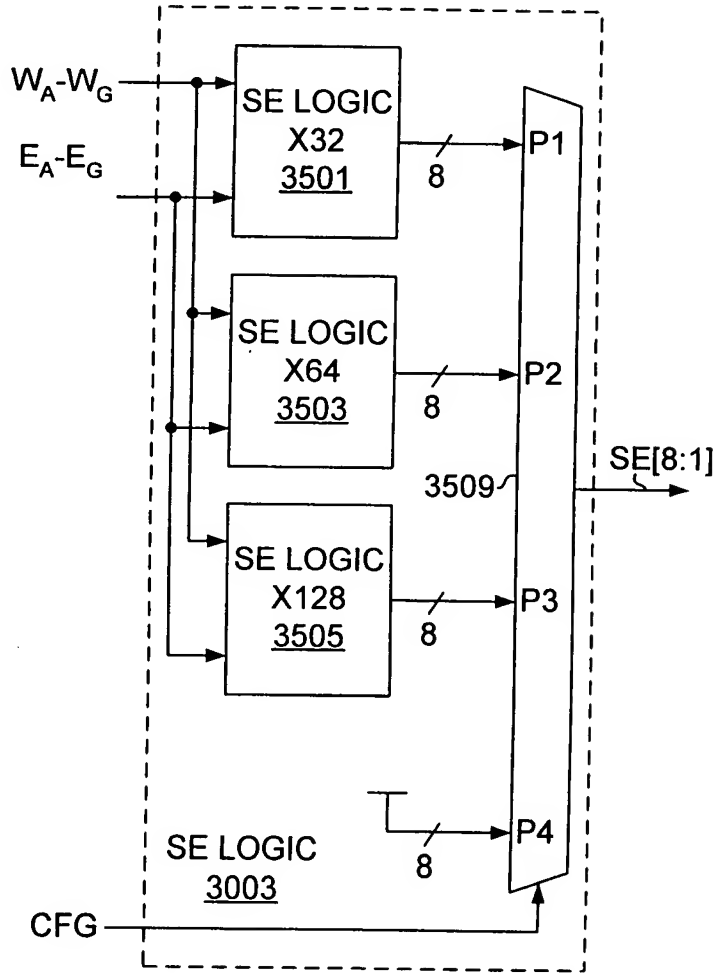


FIG. 35

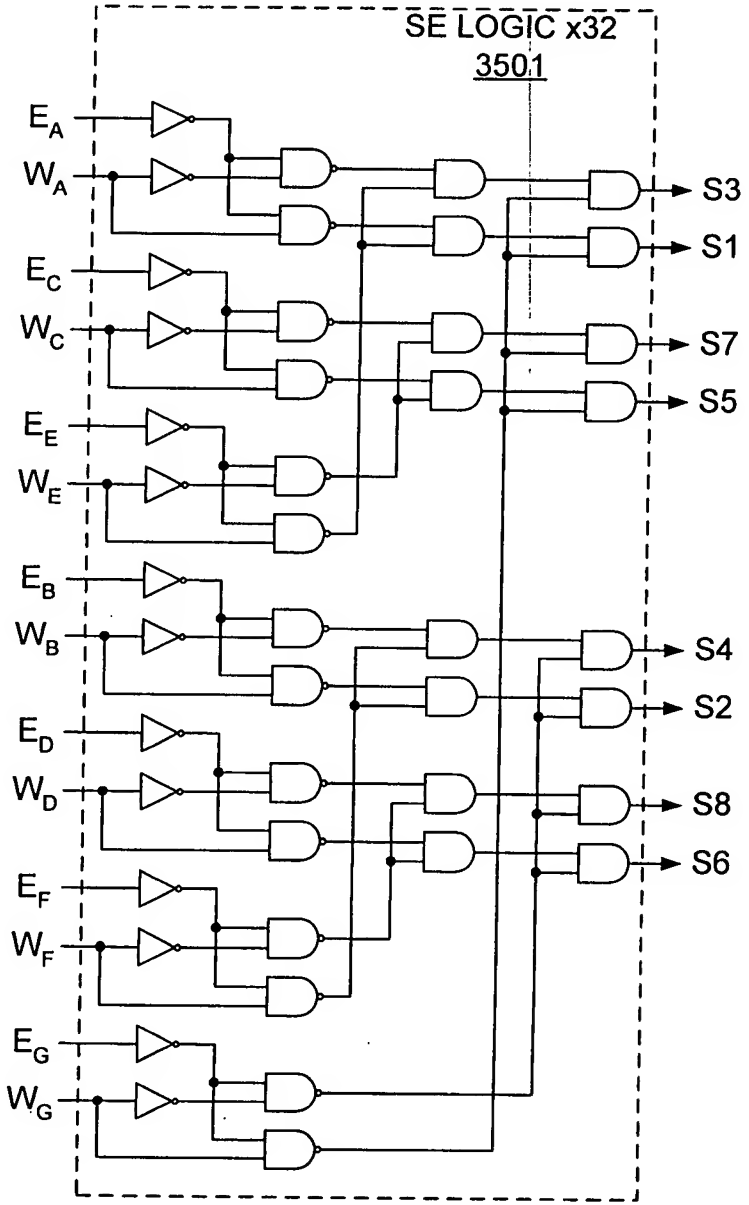


FIG. 36

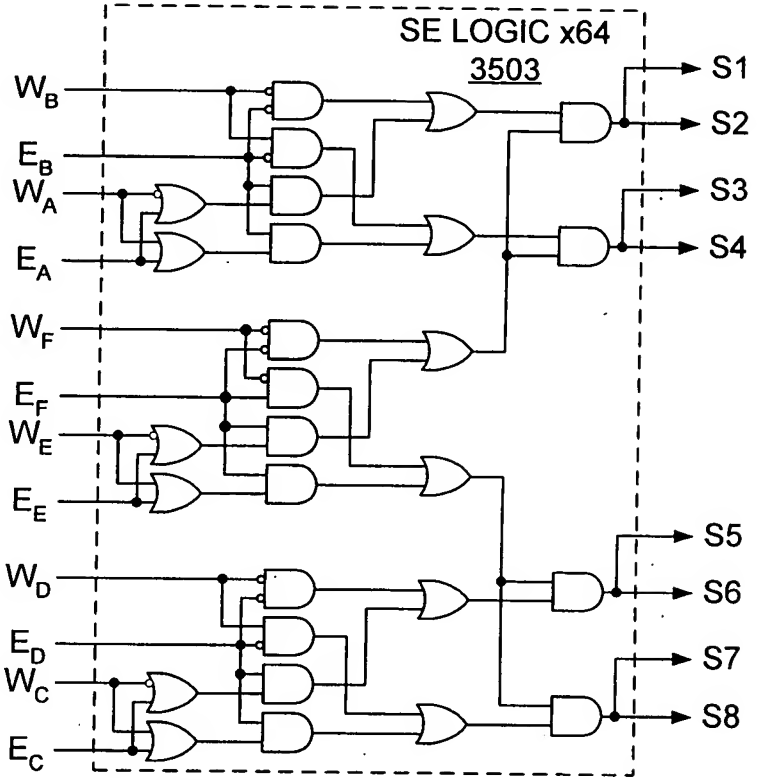
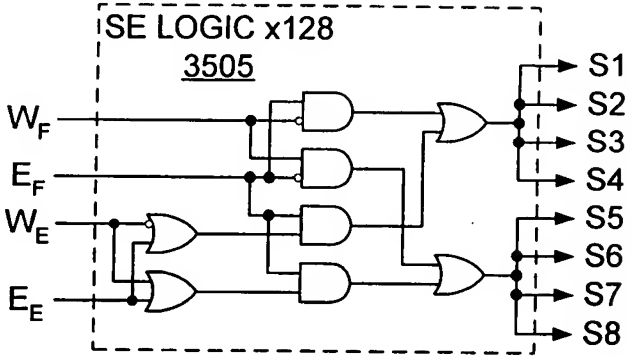


FIG. 37

FIG. 38



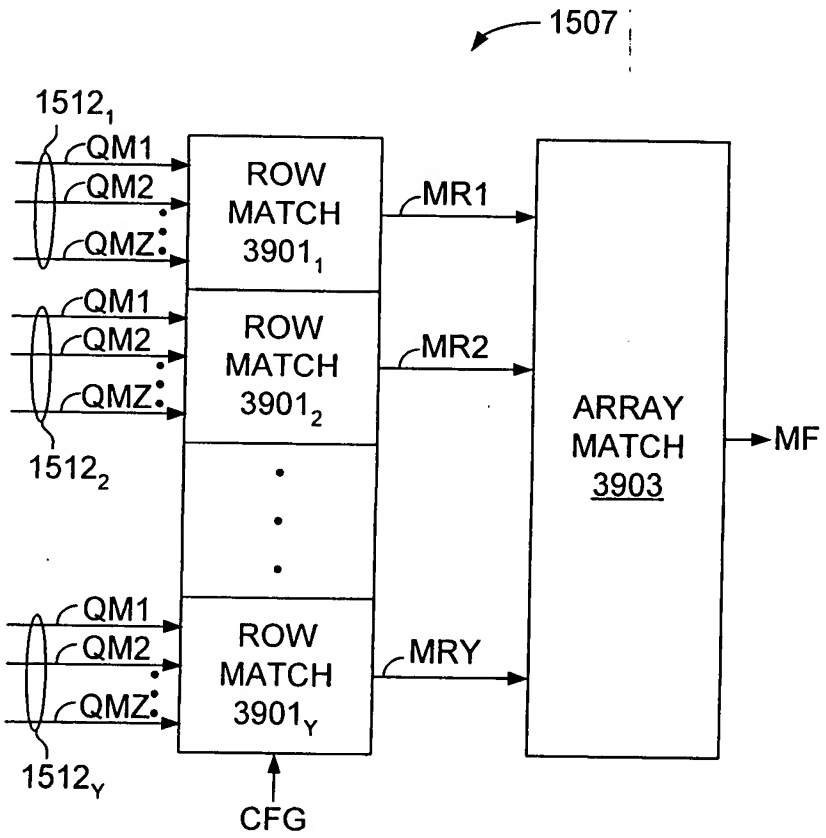

1507
1512$_1$
QM1
QM2
QMZ
ROW MATCH 3901$_1$
MR1
1512$_2$
ROW MATCH 3901$_2$
MR2
ROW MATCH 3901$_Y$
MRY
1512$_Y$
CFG
ARRAY MATCH 3903
MF

FIG. 39

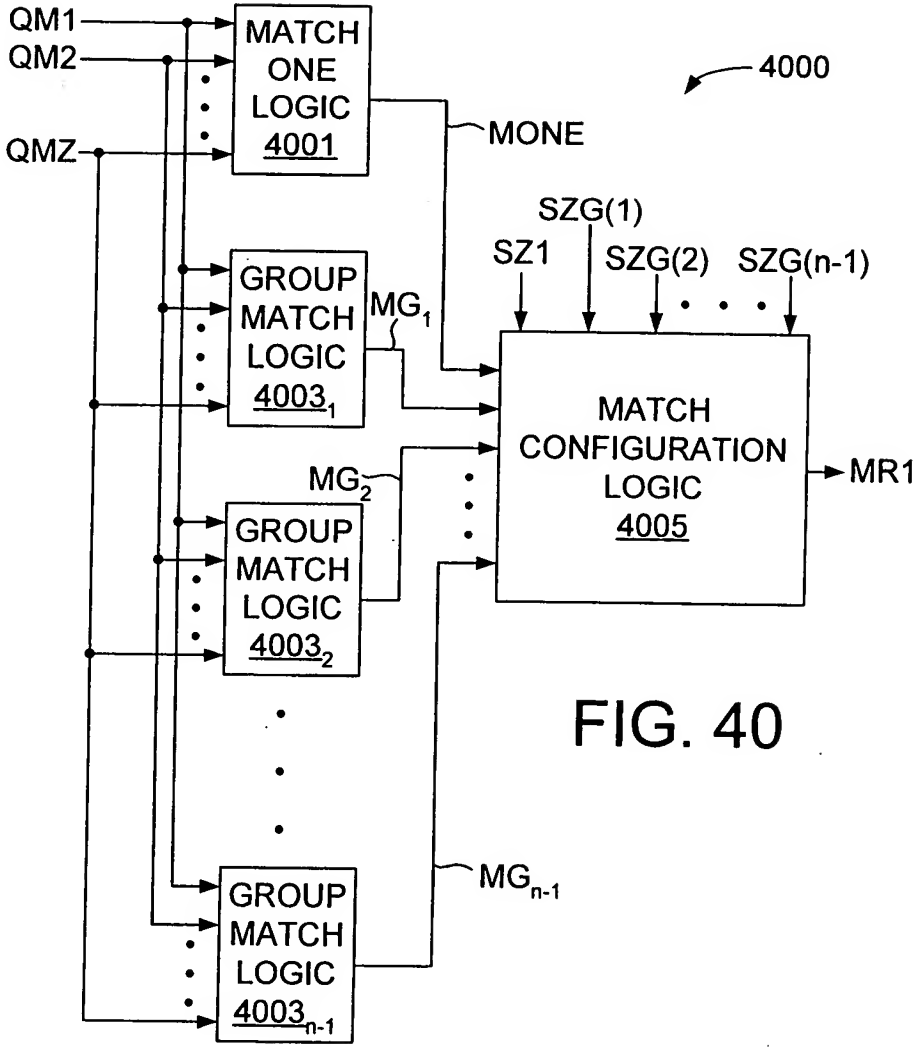

4000
QM1
QM2
QMZ
MATCH ONE LOGIC 4001
MONE
SZG(1)
SZ1
SZG(2)
SZG(n-1)
GROUP MATCH LOGIC 4003$_1$
MG$_1$
MG$_2$
GROUP MATCH LOGIC 4003$_2$
GROUP MATCH LOGIC 4003$_{n-1}$
MG$_{n-1}$
MATCH CONFIGURATION LOGIC 4005
MR1

FIG. 40

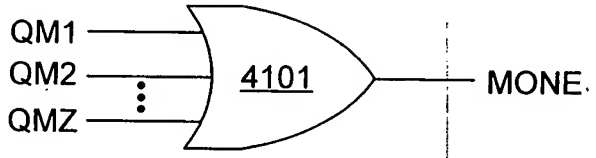


FIG. 41

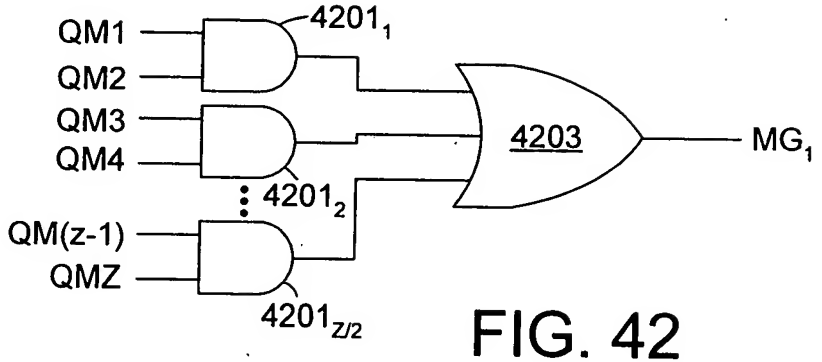


FIG. 42

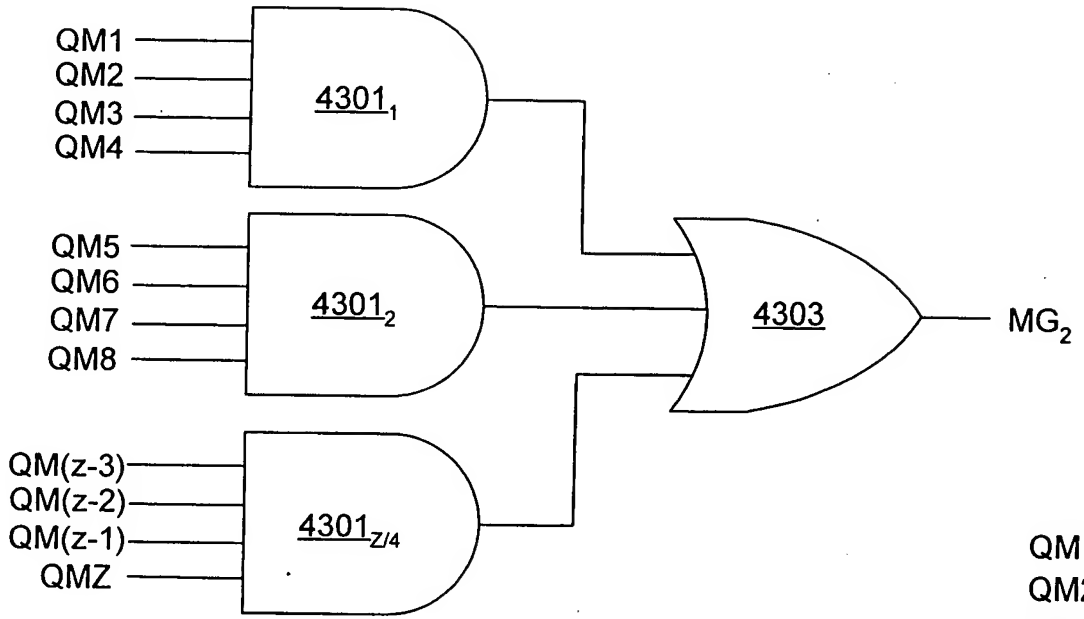


FIG. 43

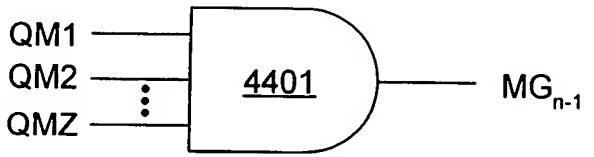


FIG. 44

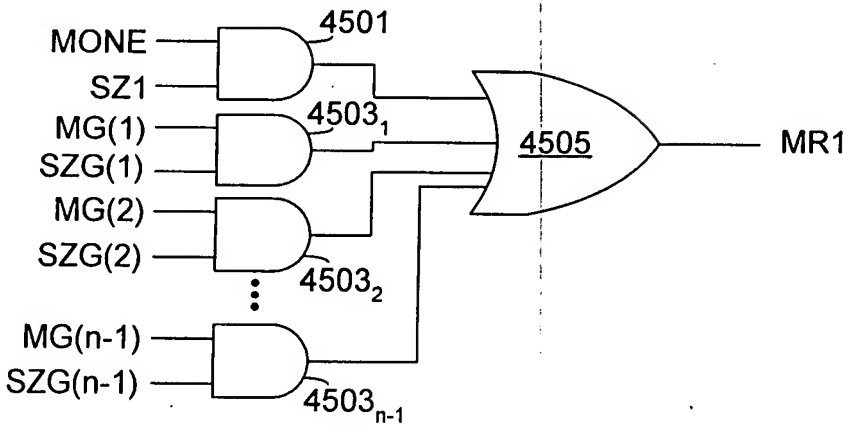

MONE
SZ1
MG(1)
SZG(1)
MG(2)
SZG(2)
MG(n-1)
SZG(n-1)
4501
4503$_1$
4503$_2$
4503$_{n-1}$
4505
MR1

FIG. 45

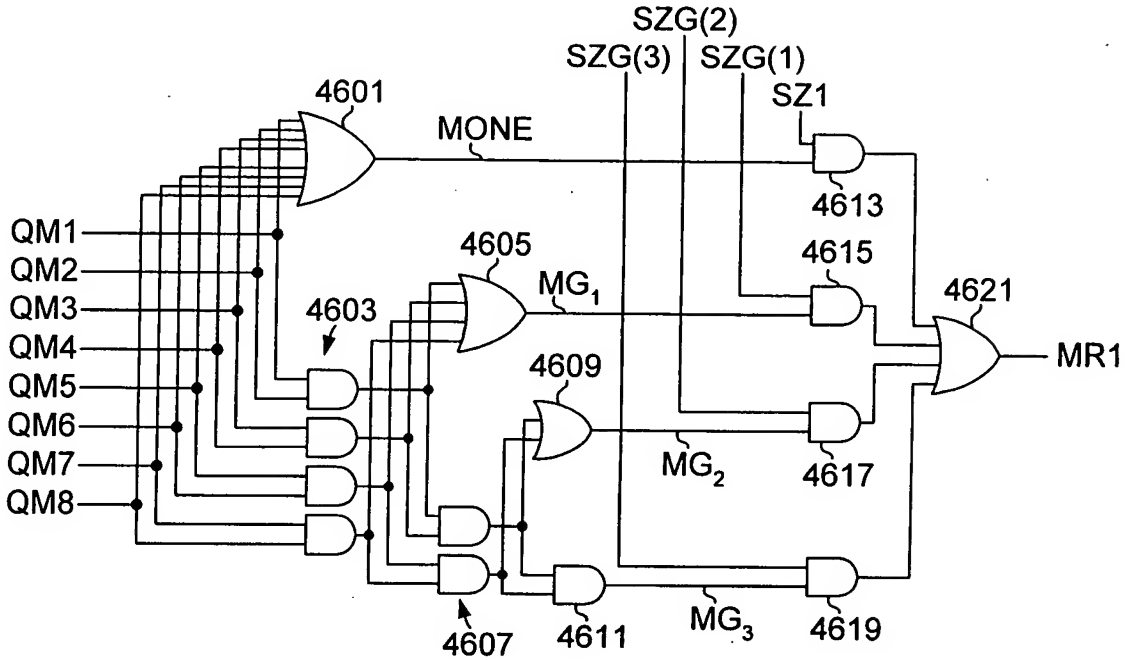

SZG(2)
SZG(3)
SZG(1)
SZ1
4601
MONE
4613
QM1
QM2
QM3
QM4
QM5
QM6
QM7
QM8
4605
MG$_1$
4615
4621
MR1
4603
4609
MG$_2$
4617
4607
4611
MG$_3$
4619

FIG. 46

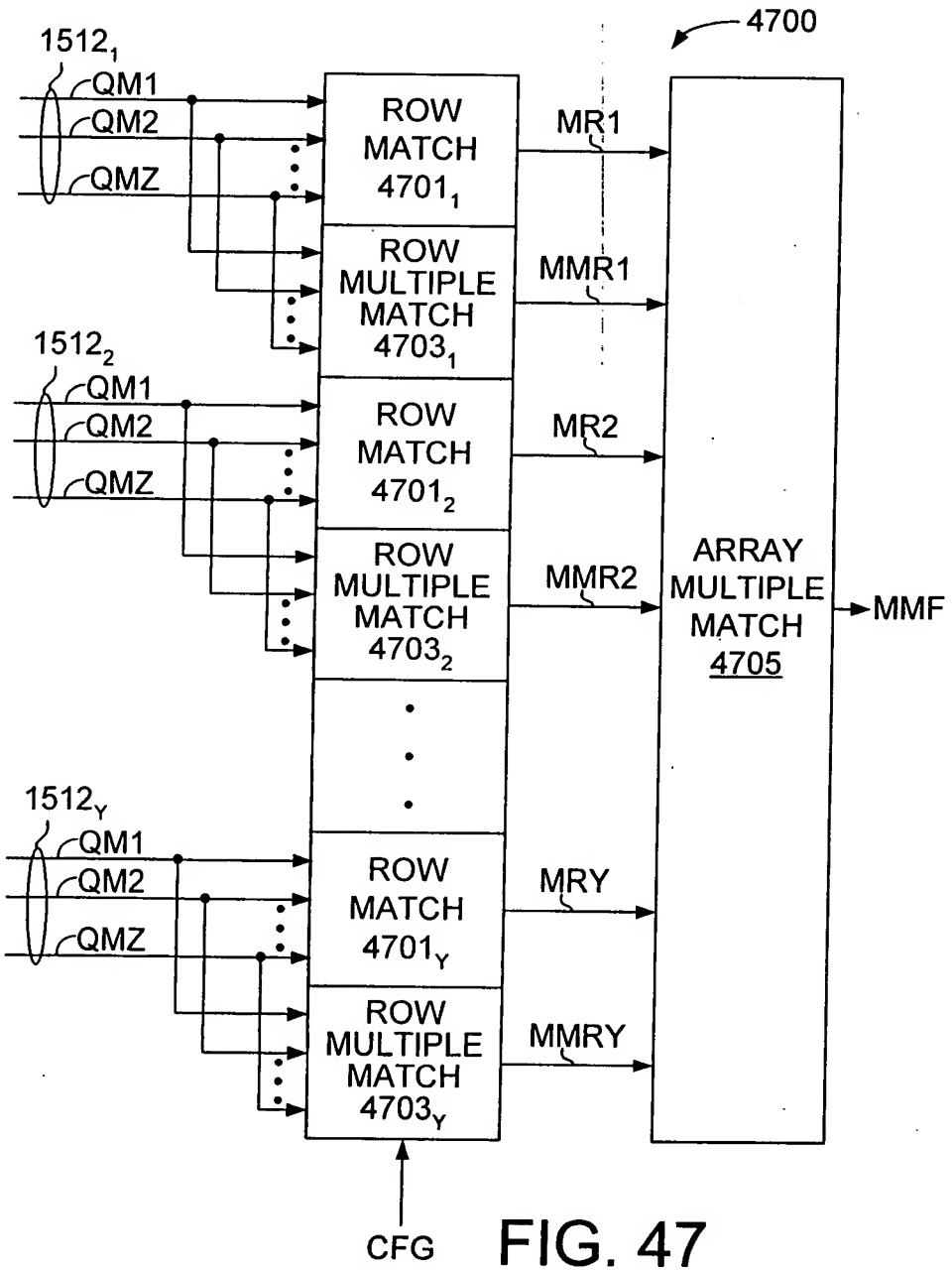

4700
1512$_1$
QM1
QM2
QMZ
ROW MATCH 4701$_1$
ROW MULTIPLE MATCH 4703$_1$
MR1
MMR1
1512$_2$
QM1
QM2
QMZ
ROW MATCH 4701$_2$
ROW MULTIPLE MATCH 4703$_2$
MR2
MMR2
ARRAY MULTIPLE MATCH 4705
MMF
1512$_Y$
QM1
QM2
QMZ
ROW MATCH 4701$_Y$
ROW MULTIPLE MATCH 4703$_Y$
MRY
MMRY
CFG

FIG. 47

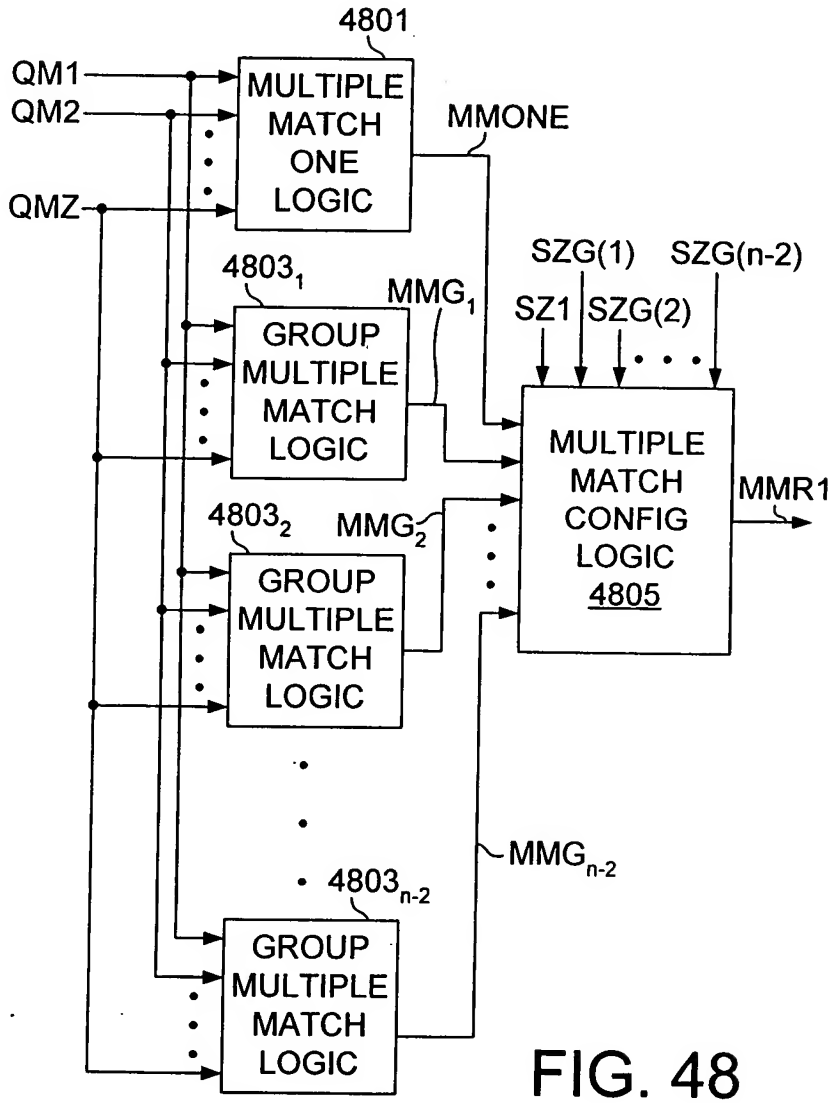

4801
QM1
QM2
QMZ
MULTIPLE MATCH ONE LOGIC
MMONE
4803$_1$
GROUP MULTIPLE MATCH LOGIC
MMG$_1$
4803$_2$
GROUP MULTIPLE MATCH LOGIC
MMG$_2$
4803$_{n-2}$
GROUP MULTIPLE MATCH LOGIC
MMG$_{n-2}$
SZG(1)
SZG(n-2)
SZ1
SZG(2)
MULTIPLE MATCH CONFIG LOGIC 4805
MMR1

FIG. 48

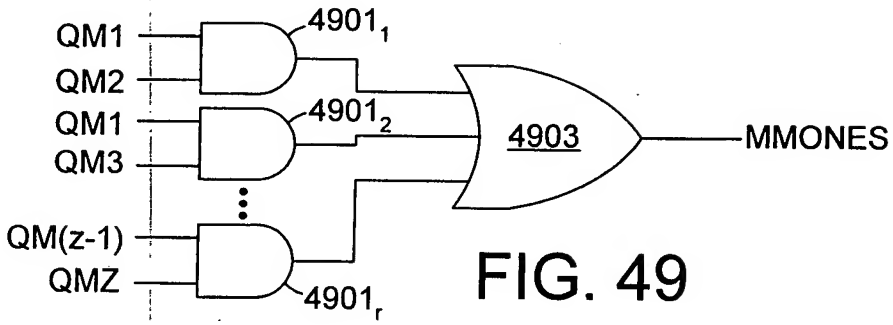

QM1
QM2
QM1
QM3
QM(z-1)
QMZ
4901$_1$
4901$_2$
4901$_r$
4903
MMONES

FIG. 49

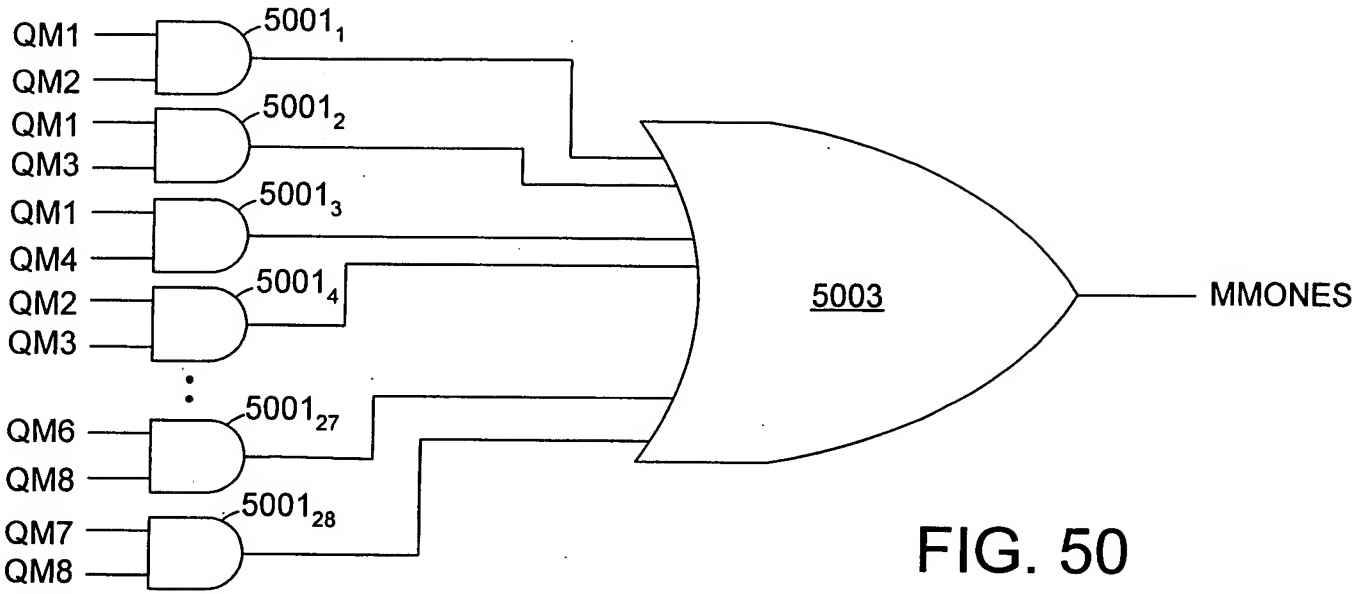

QM1
QM2
QM1
QM3
QM1
QM4
QM2
QM3
QM6
QM8
QM7
QM8
5001$_1$
5001$_2$
5001$_3$
5001$_4$
5001$_{27}$
5001$_{28}$
5003
MMONES

FIG. 50

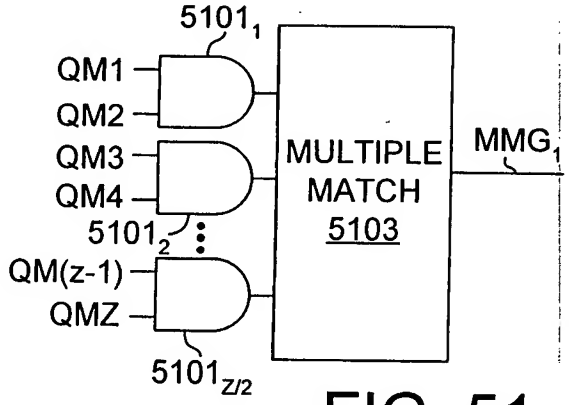


FIG. 51

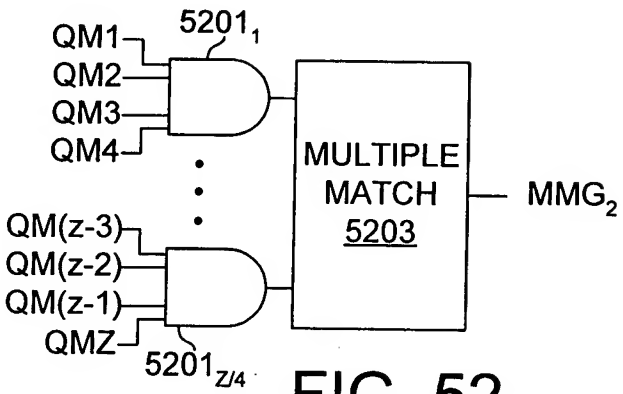


FIG. 52

FIG. 55

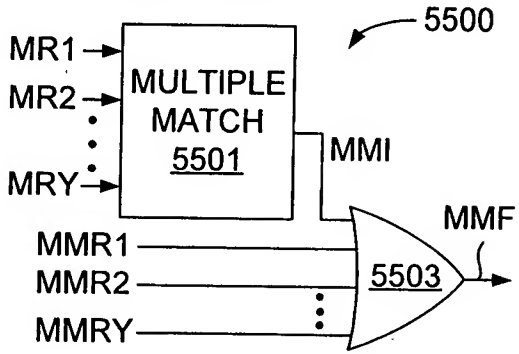


FIG. 53

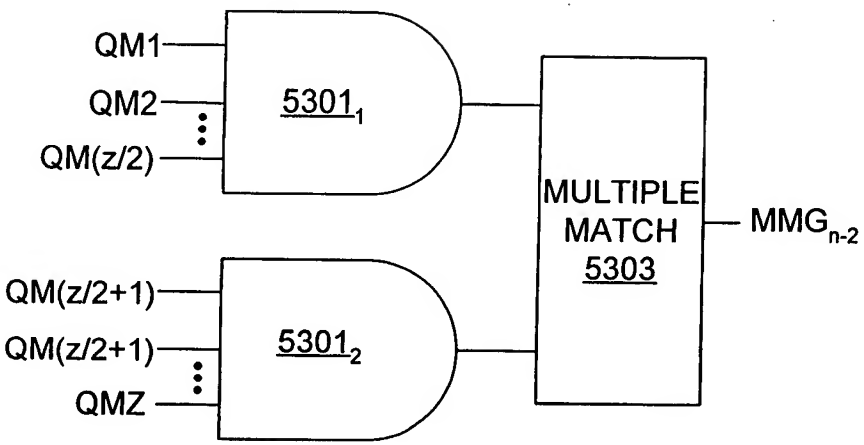
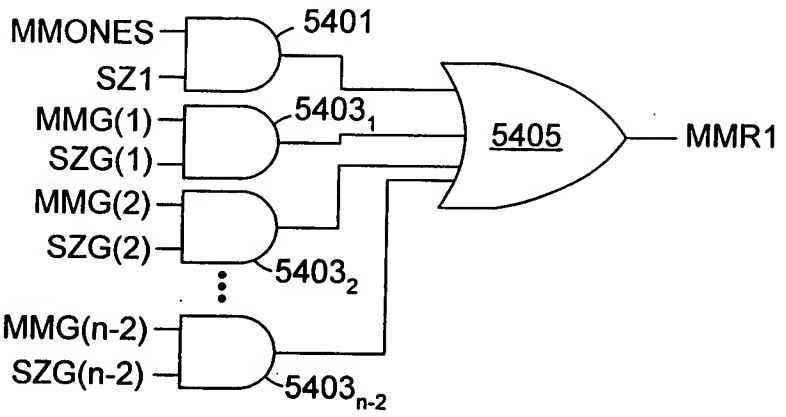


FIG. 54



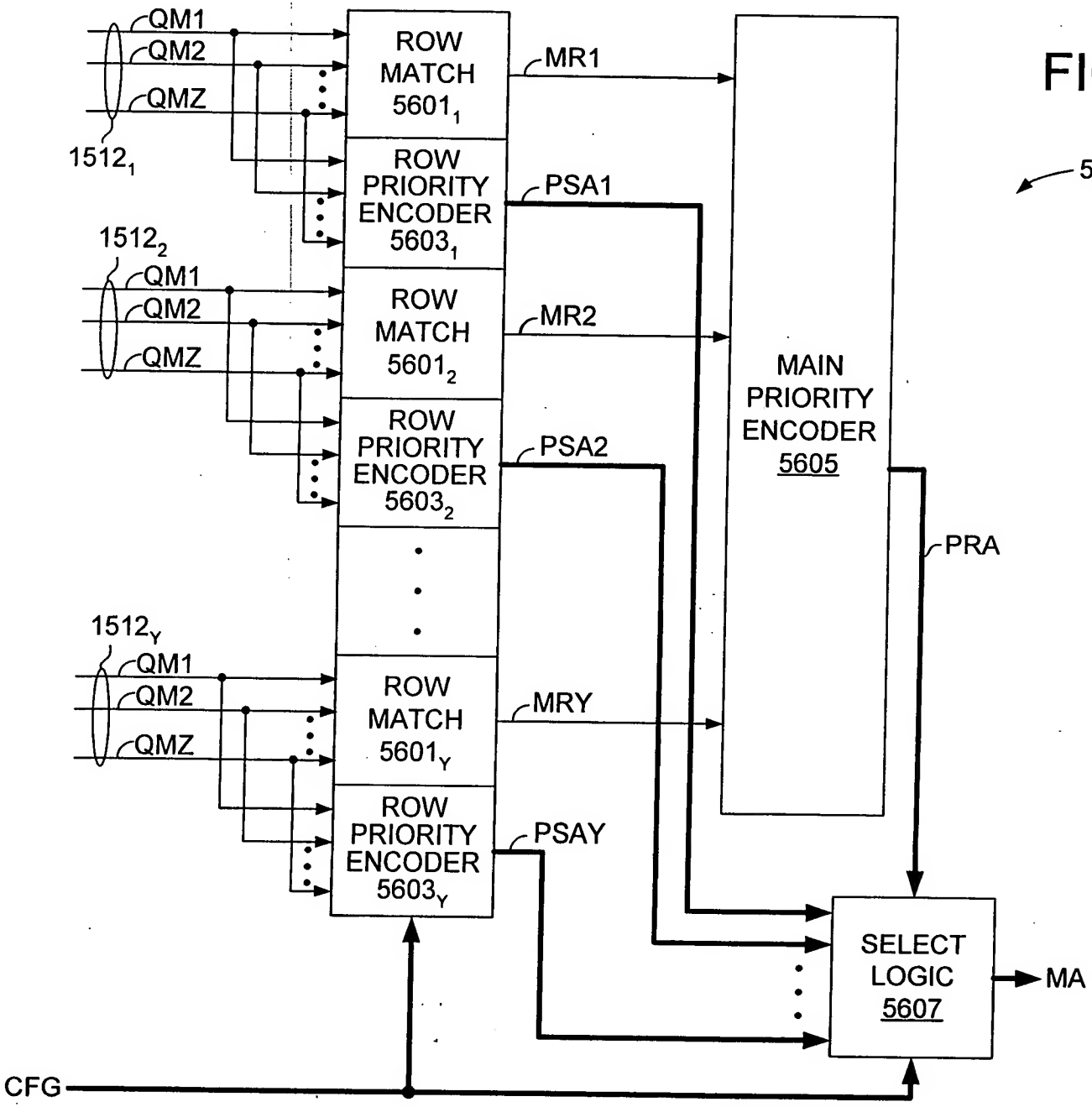

QM1
QM2
QMZ
1512$_1$
ROW MATCH 5601$_1$
ROW PRIORITY ENCODER 5603$_1$
MR1
PSA1
1512$_2$
QM1
QM2
QMZ
ROW MATCH 5601$_2$
ROW PRIORITY ENCODER 5603$_2$
MR2
PSA2
MAIN PRIORITY ENCODER 5605
PRA
1512$_Y$
QM1
QM2
QMZ
ROW MATCH 5601$_Y$
ROW PRIORITY ENCODER 5603$_Y$
MRY
PSAY
SELECT LOGIC 5607
MA
CFG
5600

FIG. 56

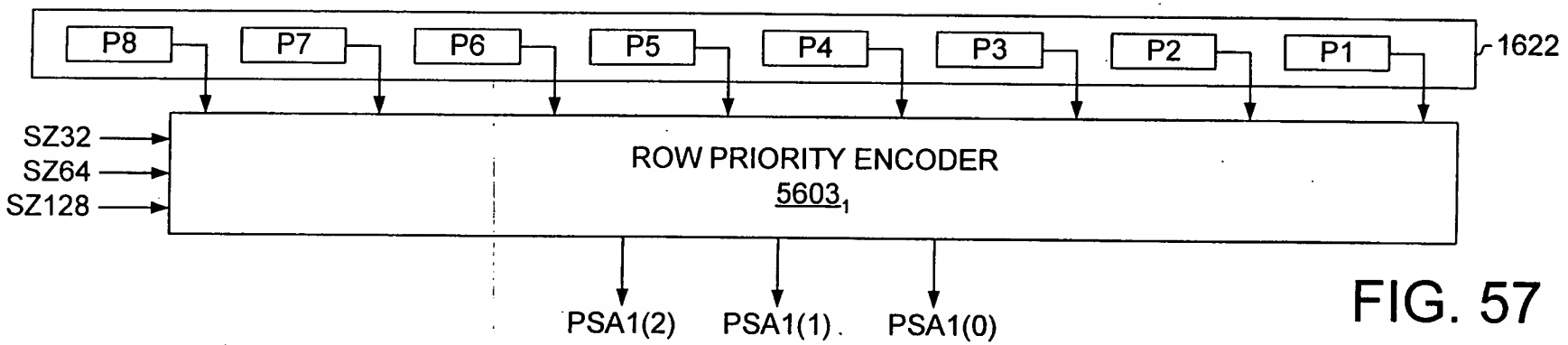


FIG. 57

QM1	QM2	QM3	QM4	QM5	QM6	QM7	QM8	ADDR	PSA1(2)	PSA1(1)	PSA1(0)
1	X	X	X	X	X	X	X	0	0	0	0
0	1	X	X	X	X	X	X	1	0	0	1
0	0	1	X	X	X	X	X	2	0	1	0
0	0	0	1	X	X	X	X	3	0	1	1
0	0	0	0	1	X	X	X	4	1	0	0
0	0	0	0	0	1	X	X	5	1	0	1
0	0	0	0	0	0	1	X	6	1	1	0
0	0	0	0	0	0	0	1	7	1	1	1
0	0	0	0	0	0	0	0	X	X	X	X

SZ32

QM1●QM2	QM3●QM4	QM5●QM6	QM7●QM8	ADDR	PSA1(2)	PSA1(1)	PSA1(0)
1	X	X	X	0	0	0	X
0	1	X	X	1	0	1	X
0	0	1	X	2	1	0	X
0	0	0	1	3	1	1	X
0	0	0	0	X	X	X	X

SZ64

QM1●QM2●QM3●QM4	QM5●QM6●QM7●QM8	ADDR	PSA1(2)	PSA1(1)	PSA1(0)
1	X	0	0	X	X
0	1	1	1	X	X
0	0	X	X	X	X

SZ128

CFG

FIG. 58

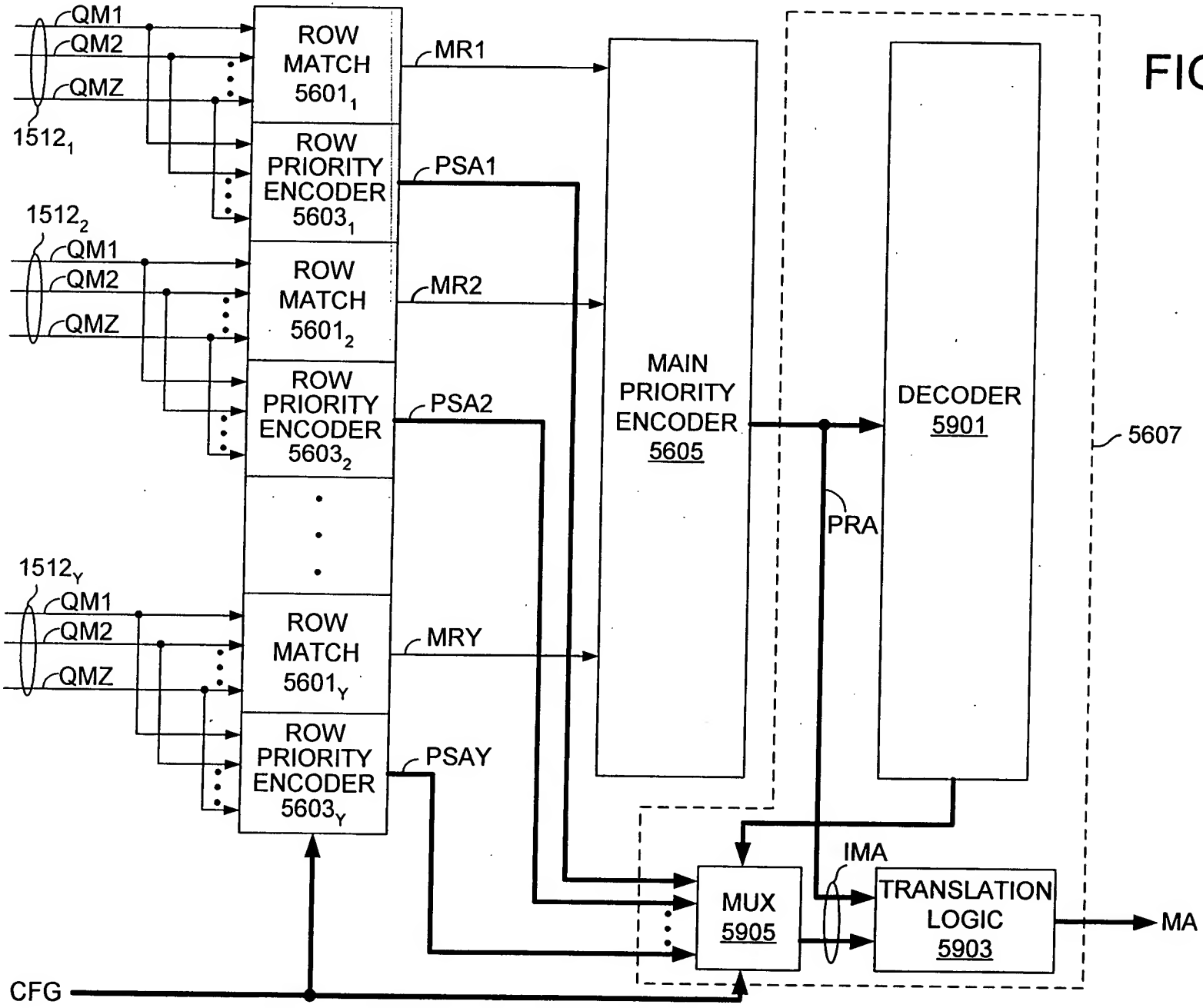

QM1
QM2
QMZ
1512$_1$
ROW MATCH 5601$_1$
ROW PRIORITY ENCODER 5603$_1$
MR1
PSA1
1512$_2$
QM1
QM2
QMZ
ROW MATCH 5601$_2$
ROW PRIORITY ENCODER 5603$_2$
MR2
PSA2
1512$_Y$
QM1
QM2
QMZ
ROW MATCH 5601$_Y$
ROW PRIORITY ENCODER 5603$_Y$
MRY
PSAY
MAIN PRIORITY ENCODER 5605
DECODER 5901
5607
PRA
IMA
MUX 5905
TRANSLATION LOGIC 5903
MA
CFG

FIG. 59

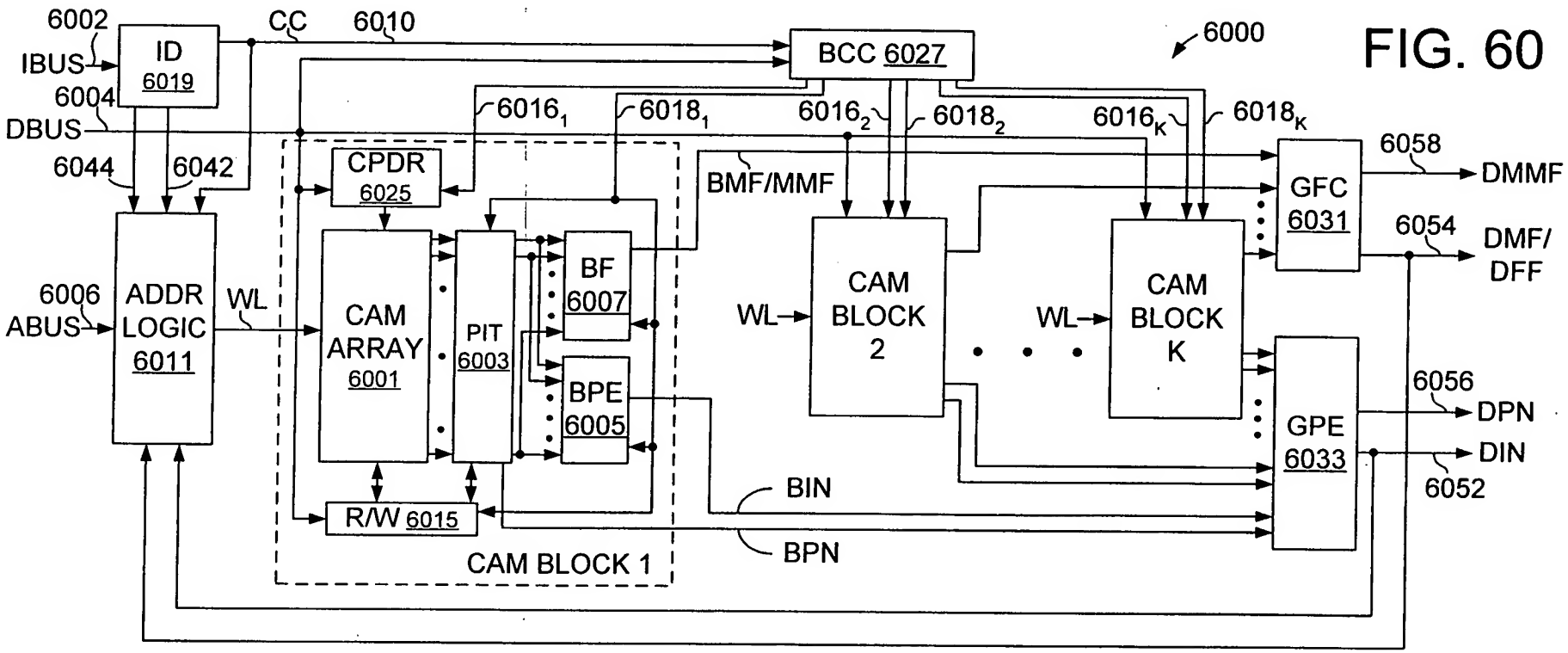


FIG. 60

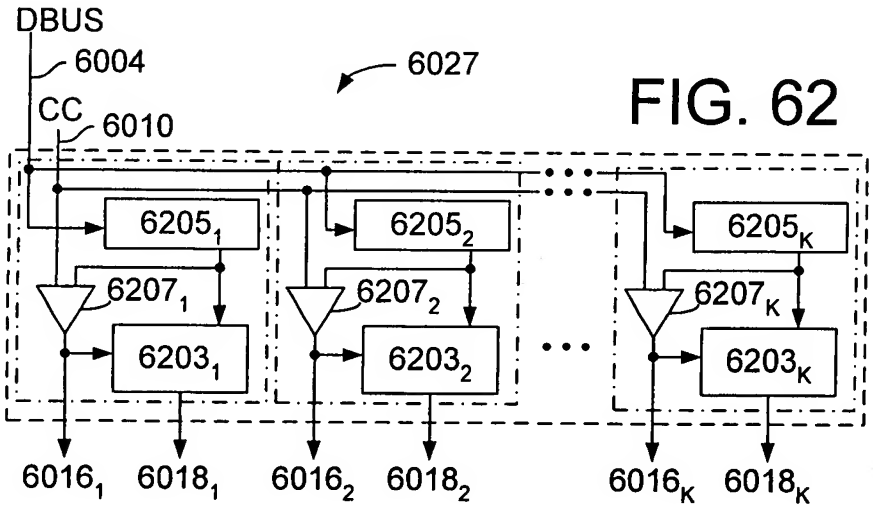


FIG. 62

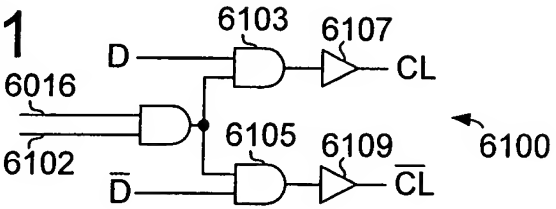


FIG. 61

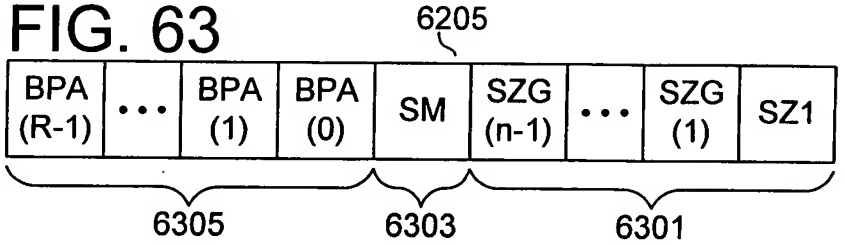


FIG. 63

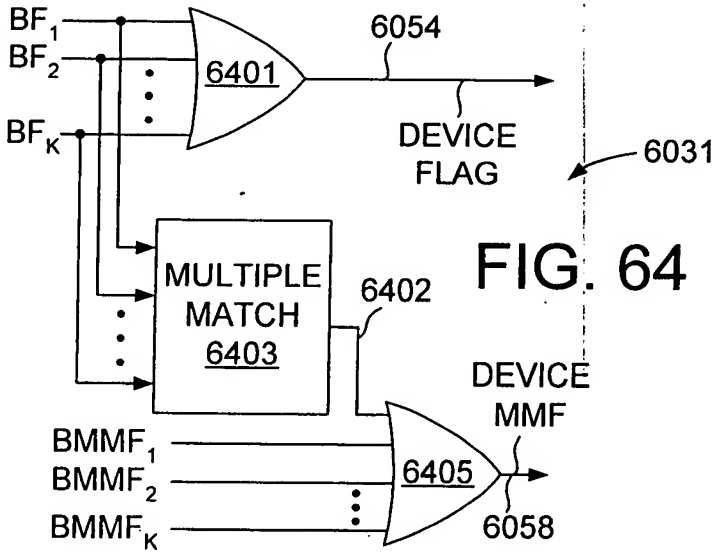


FIG. 64

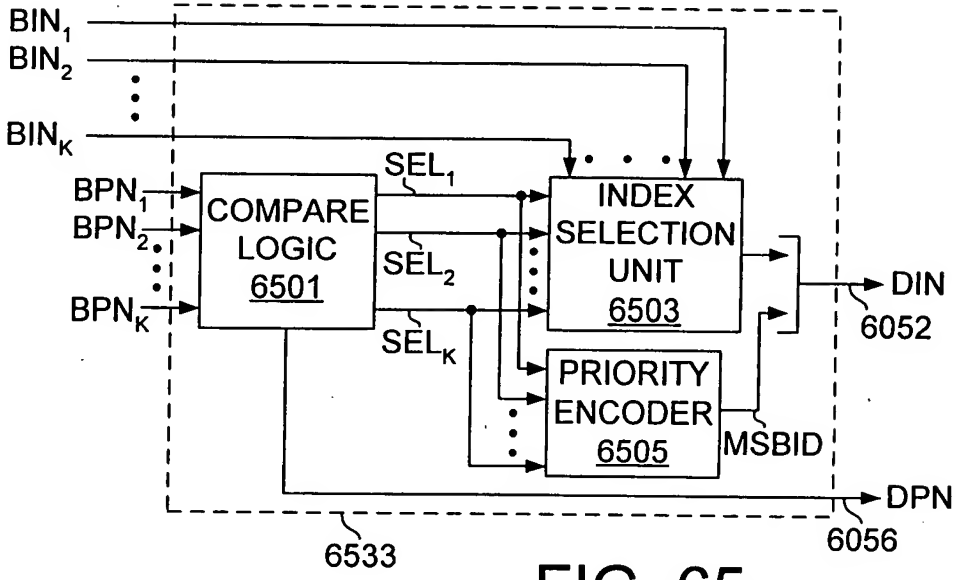


FIG. 65

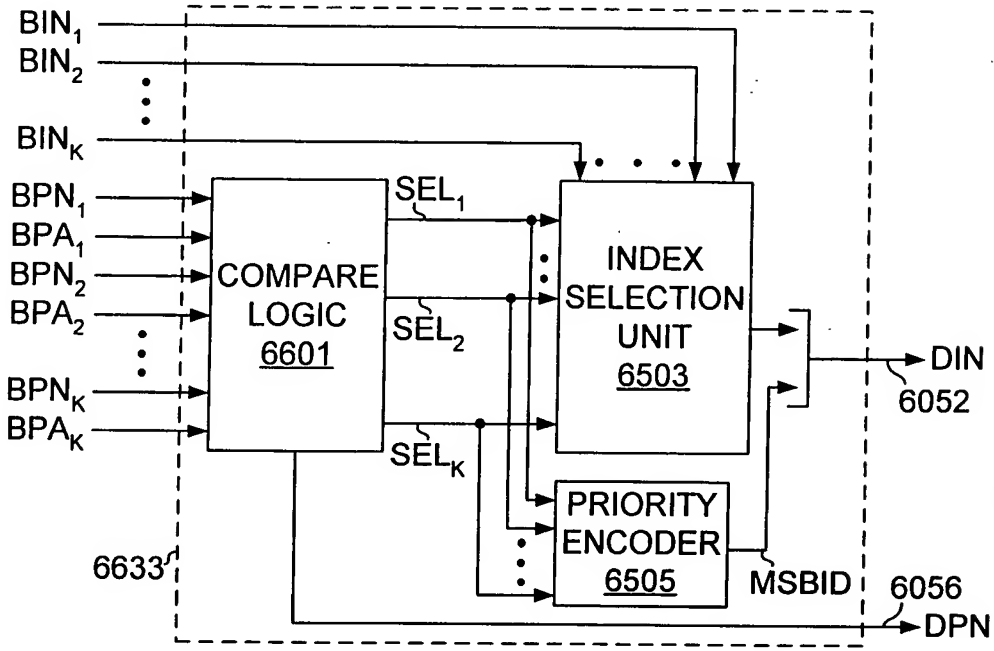


FIG. 66

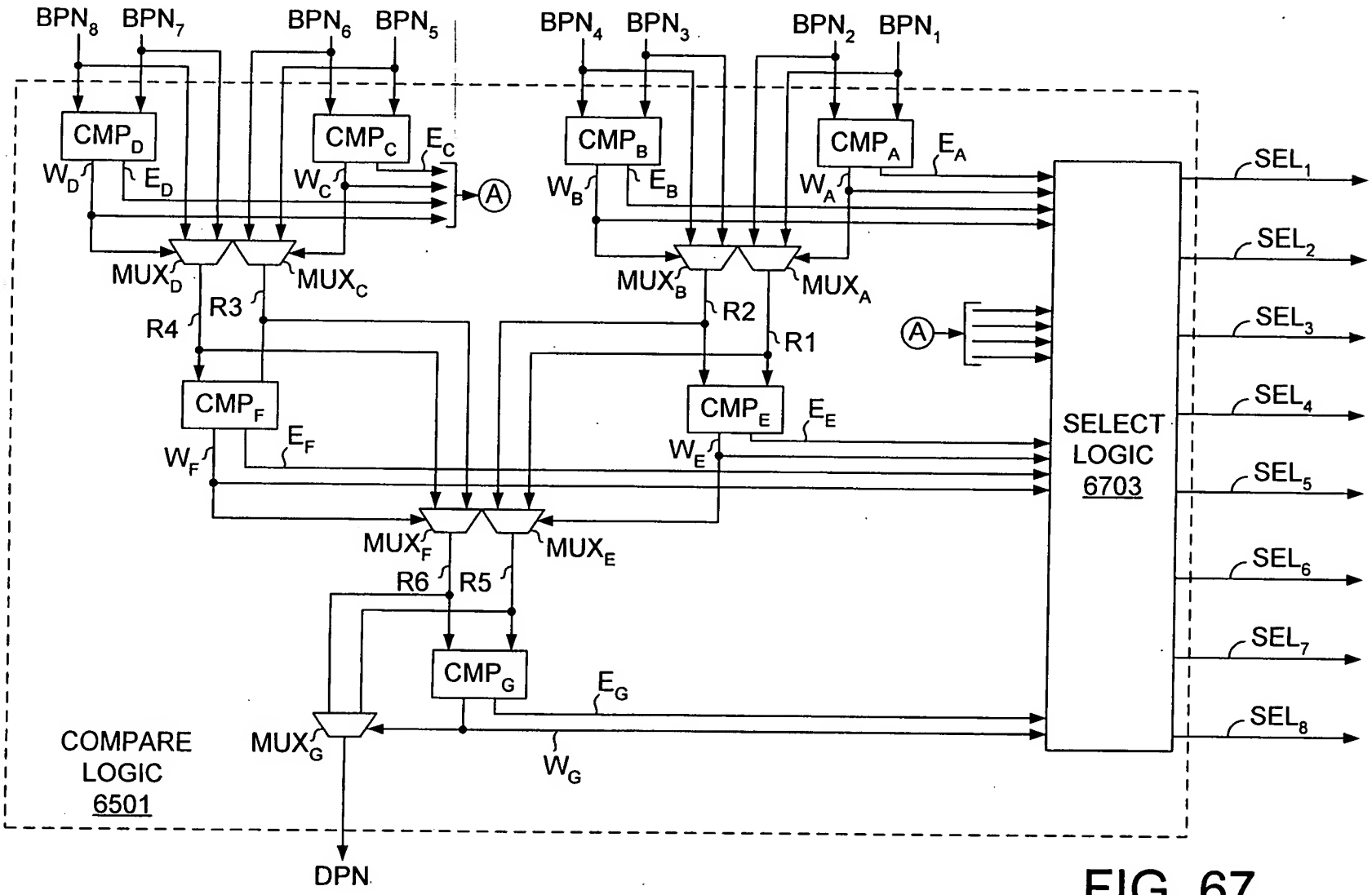

BPN8
BPN7
BPN6
BPN5
BPN4
BPN3
BPN2
BPN1
CMPD
CMPC
CMPB
CMPA
CMPF
CMPE
CMPG
WD
ED
WC
EC
WB
EB
WA
EA
WF
EF
WE
EE
WG
EG
MUXD
MUXC
MUXB
MUXA
MUXF
MUXE
MUXG
R1
R2
R3
R4
R5
R6
A
SELECT LOGIC 6703
SEL1
SEL2
SEL3
SEL4
SEL5
SEL6
SEL7
SEL8
COMPARE LOGIC 6501
DPN

FIG. 67

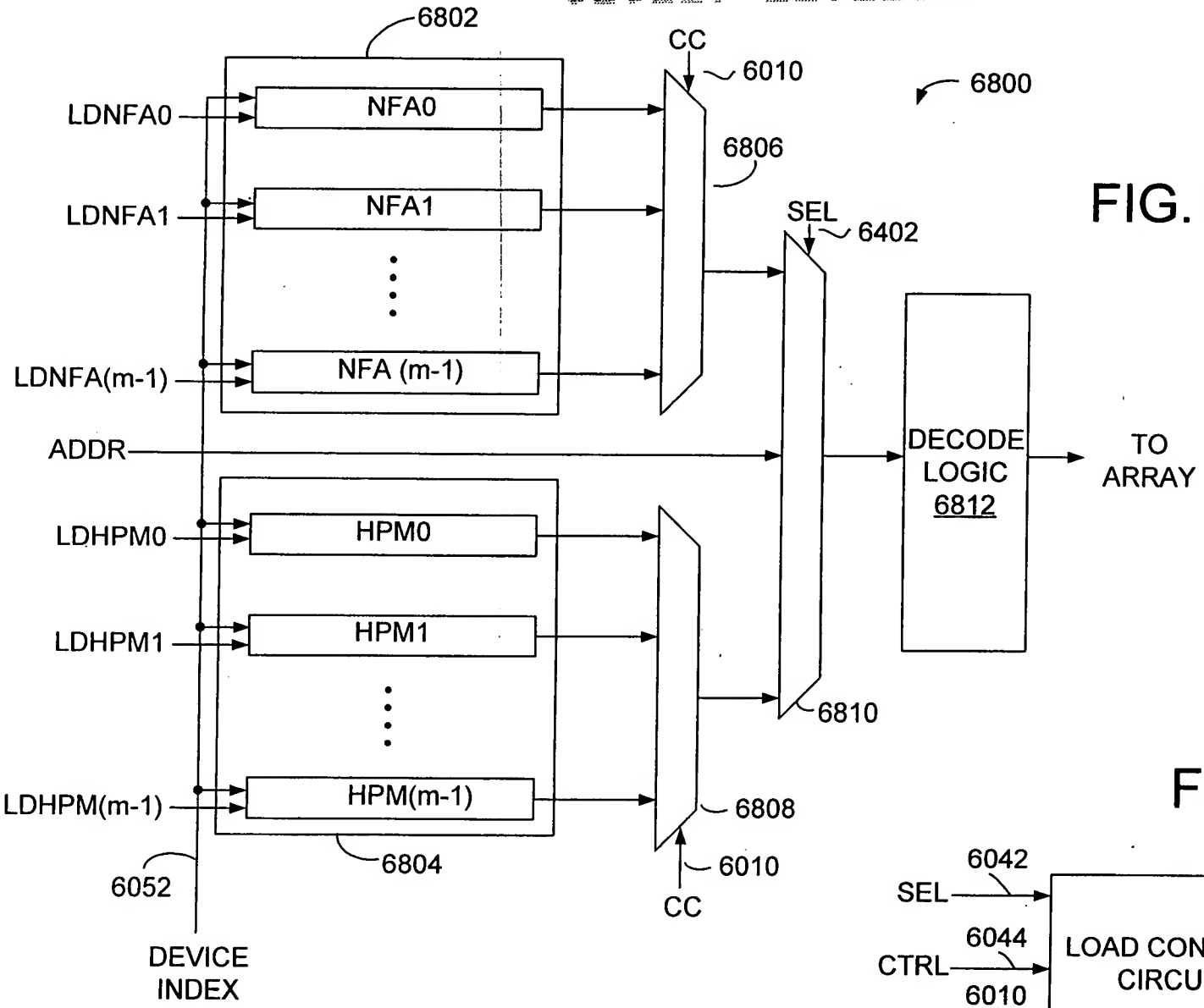

6802
CC
6010
6800
LDNFA0
NFA0
6806
LDNFA1
NFA1
SEL
6402
LDNFA(m-1)
NFA (m-1)
ADDR
DECODE LOGIC 6812
TO ARRAY
LDHPM0
HPM0
LDHPM1
HPM1
6810
LDHPM(m-1)
HPM(m-1)
6808
6804
6010
6052
CC
DEVICE INDEX

FIG. 68

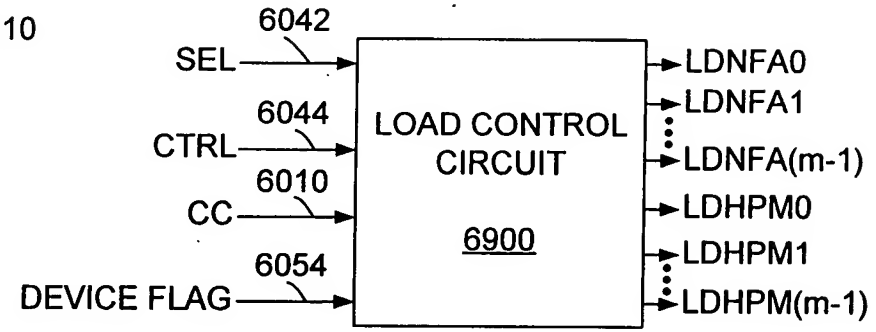

6042
SEL
6044
CTRL
6010
CC
6054
DEVICE FLAG
LOAD CONTROL CIRCUIT
6900
LDNFA0
LDNFA1
LDNFA(m-1)
LDHPM0
LDHPM1
LDHPM(m-1)

FIG. 69

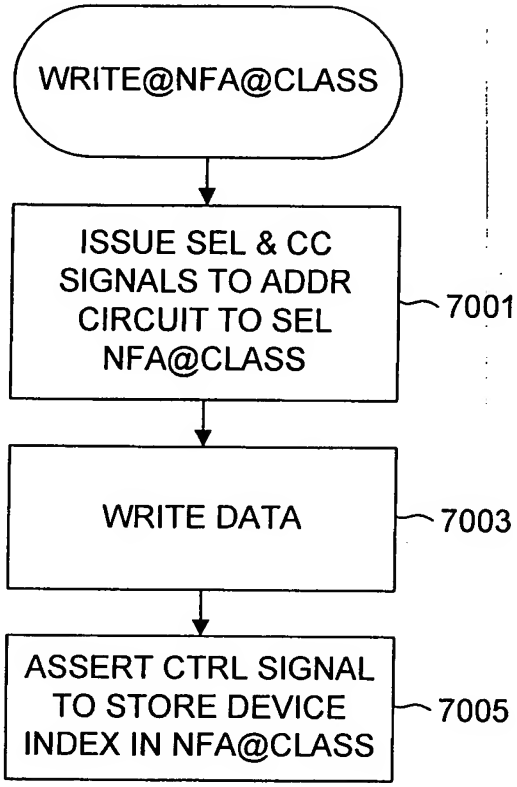


FIG. 70

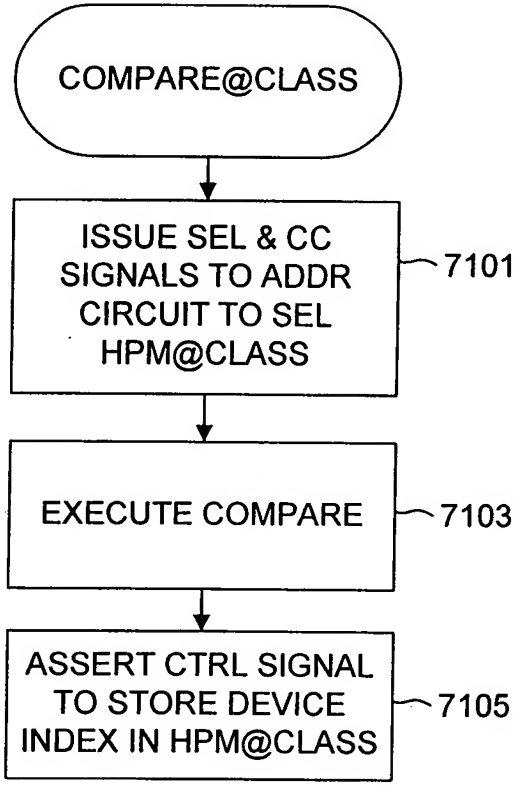


FIG. 71

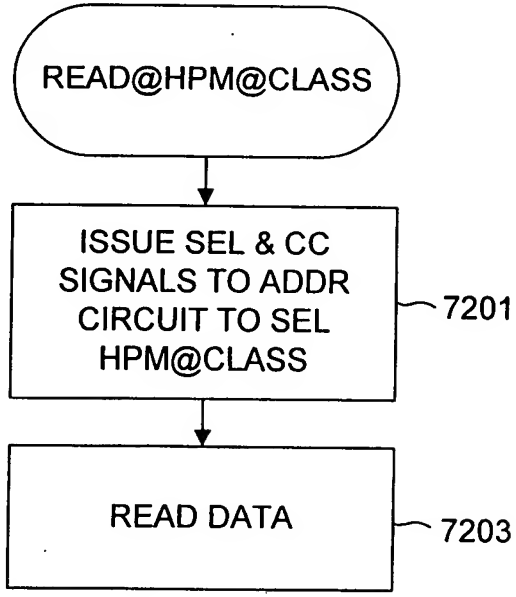


FIG. 72

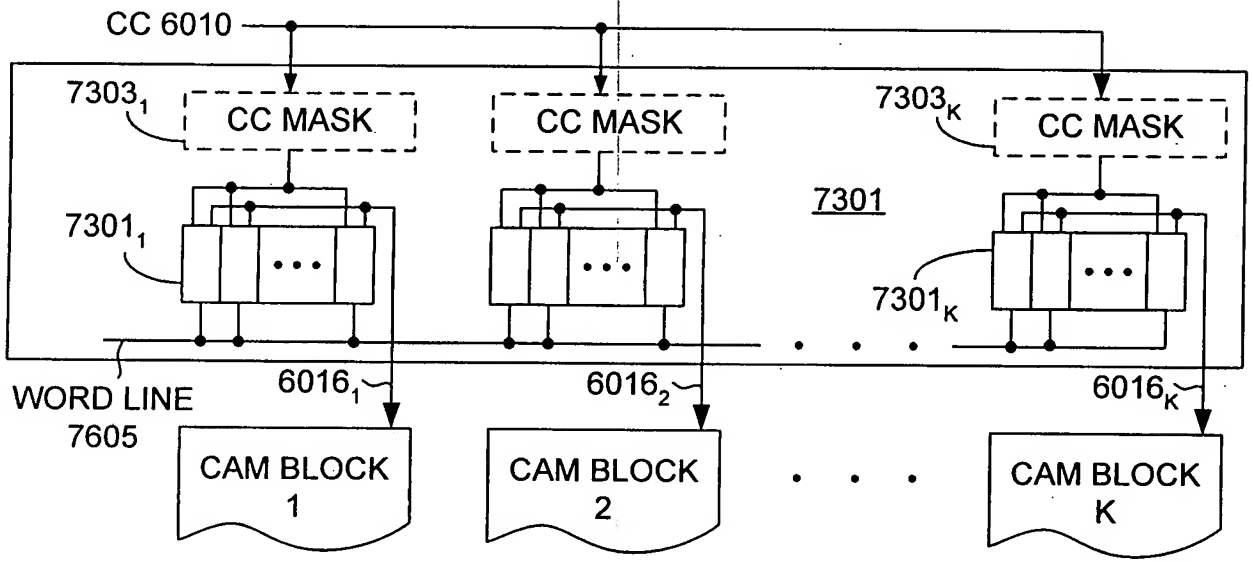

CC 6010
7303$_1$
CC MASK
CC MASK
7303$_K$
CC MASK
7301
7301$_1$
7301$_K$
WORD LINE
7605
6016$_1$
6016$_2$
6016$_K$
CAM BLOCK 1
CAM BLOCK 2
CAM BLOCK K

FIG. 73

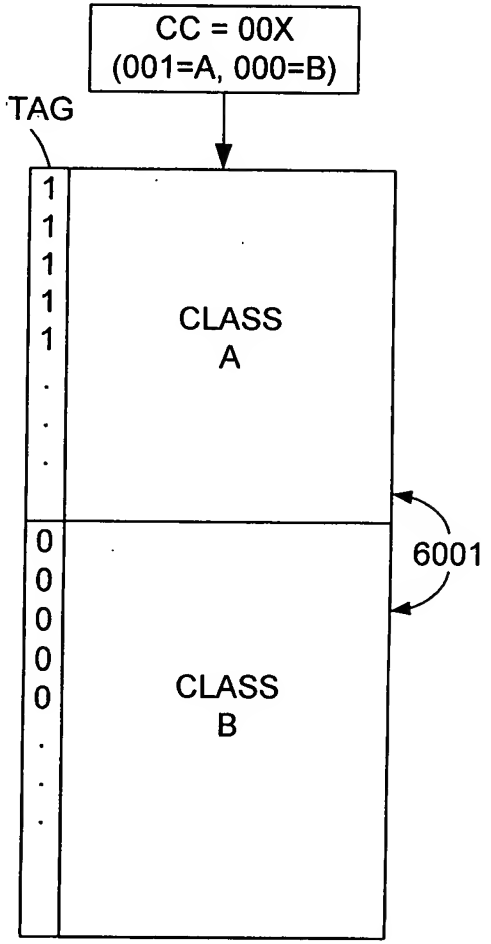

CC = 00X
(001=A, 000=B)
TAG
1
1
1
1
1
CLASS A
0
0
0
0
0
CLASS B
6001

FIG. 74

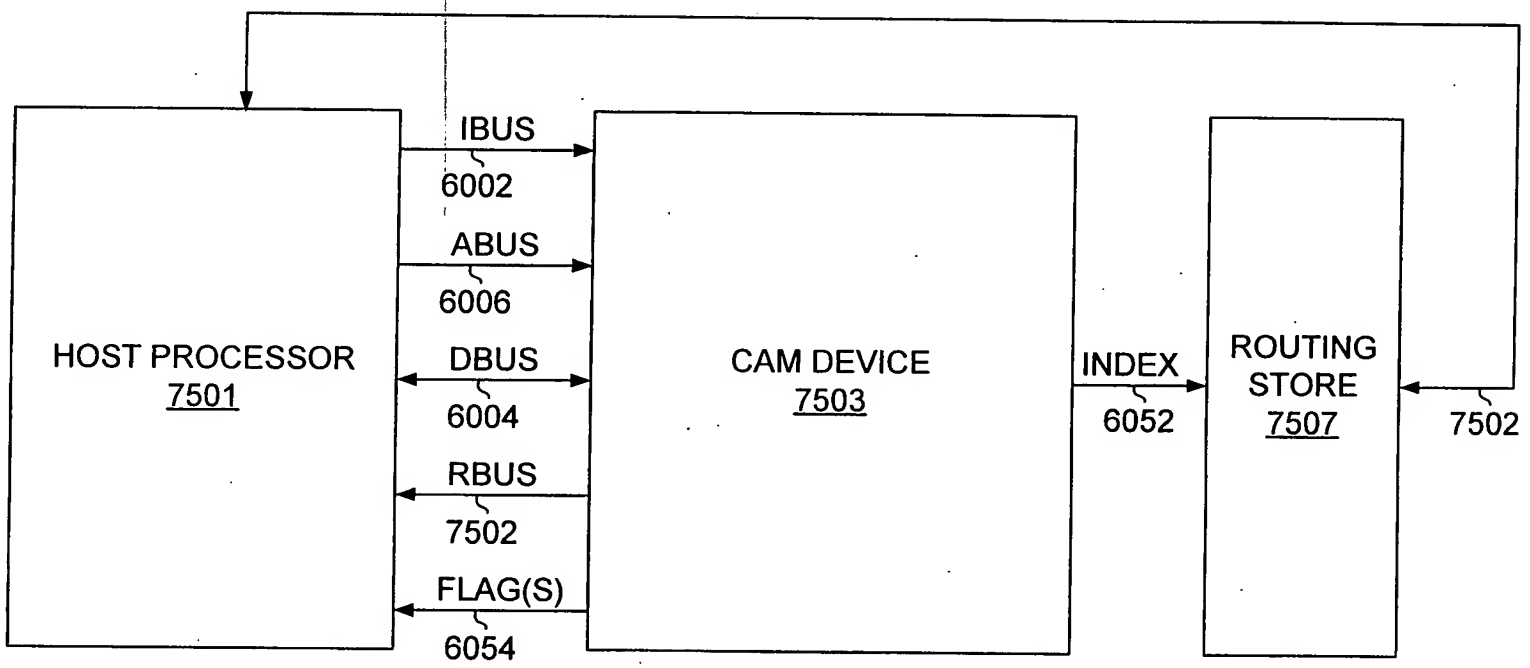

HOST PROCESSOR
7501
IBUS
6002
ABUS
6006
DBUS
6004
RBUS
7502
FLAG(S)
6054
CAM DEVICE
7503
INDEX
6052
ROUTING
STORE
7507
7502
7500

FIG. 75